Datasheet

APM32E030x8

Arm® Cortex® -M0+ -based 32-bit MCU

Version: V1.1

1 Product Characteristics

- **System Architecture**
  - 32-bit Arm® Cortex®-M0+ core
  - 72MHz working frequency
- **Memory**
  - Flash: The capacity is 64KB
  - SRAM: The capacity is 8KB
- **Clock**
  - HSECLK: 4~32MHz external crystal/ceramic oscillator supported
  - LSECLK: 32.768KHz crystal/ceramic oscillator supported
  - HSICLK: 8MHz RC oscillator calibrated by factory
  - LSICLK: 40KHz RC oscillator supported
  - PLL: Phase locked loop; 2~16 frequency doubling supported
- **Reset and power management**
  - V_{DD} range: 2.0～3.6V
  - V_{DDA} range: V_{DD}～3.6V
  - Power-on/power-down reset (POR/PDR) supported
- **Low-power mode**
  - Sleep, stop and standby modes supported
- **DMA**
  - A DMA with 5 channels
- **Debugging interface**
  - SWD
- **I/O**
  - Up to 55 I/O
  - All I/O can be mapped to external interrupt vector
  - Up to 36 FT input I/O
- **Communication peripherals**
  - 2 I2C interface (1Mbit/s), supporting SMBus/PMBus
  - 2 USART interface, maximum speed is 6Mbit/s
  - 2 SPI, maximum transmission speed is 18Mbit/s
- **Analog peripherals**
  - 3 12-bit ADCs, 18 channels in 16+2 supported
- **Timer**
  - 1 16-bit advanced timers TMR1 that can provide 7-channel PWM output, support dead zone generation and braking input functions
  - 5 16-bit general-purpose timers TMR3/14/15/16/17, with independent channels to support input capture, output comparison, PWM, pulse count and other functions
  - 1 16-bit basic timers TMR6
  - 2 watchdog timers: one independent watchdog IWDT and one window watchdog WWDT
  - 1 24-bit autodecrement SysTick Timer
- **RTC**
  - Support calendar function
  - Alarm and regular wake-up from halt/standby mode
- **CRC computing unit**
- **96-bit unique device ID**
- **Chip package**
  - TSSOP20/QFN28/QFN32/QFN48/ LQFP32/LQFP48/LQFP64

Contents

2 Product Information

See the following table for APM32E030x8 product functions and peripheral configuration.

Table 1 Functions and Peripherals of APM32E030x8 Series Chips

Product		**APM32E030x8**						
Model		F8P6	G8U6	K8U6	K8T6	C8U6	C8Tx	R8T6
Package		TSSOP20	QFN28	QFN32	LQFP32	QFN48	LQFP48	LQFP64
Core and maximum working frequency		Arm® 32-bit Cortex®-M0+@72MHz						
Working voltage		2.0~3.6V						
Flash(KB)		64						
SRAM(KB)		8						
GPIOs		15	23	27	25	39		55
Communication interface	USART	1	2					
	SPI	1				2		
	I2C	0	1			2		
Timer	16-bit advanced	1						
	16-bit general	5						
	16-bit basic	1						
	System tick timer	1						
	Watchdog	2						
Real-time clock		1						
12-bit ADC	Unit	1						
	External channel	9	10					16
	Internal channel	2						
Operating temperature		Ambient temperature: -40°C to 85°C/ -40℃ to 105℃ Junction temperature: -40℃ to 105℃/ -40℃ to 125℃						

3 Pin Information

3.1 Pin distribution

Figure 1 Distribution Diagram of APM32E030x8 Series LQFP64 Pins

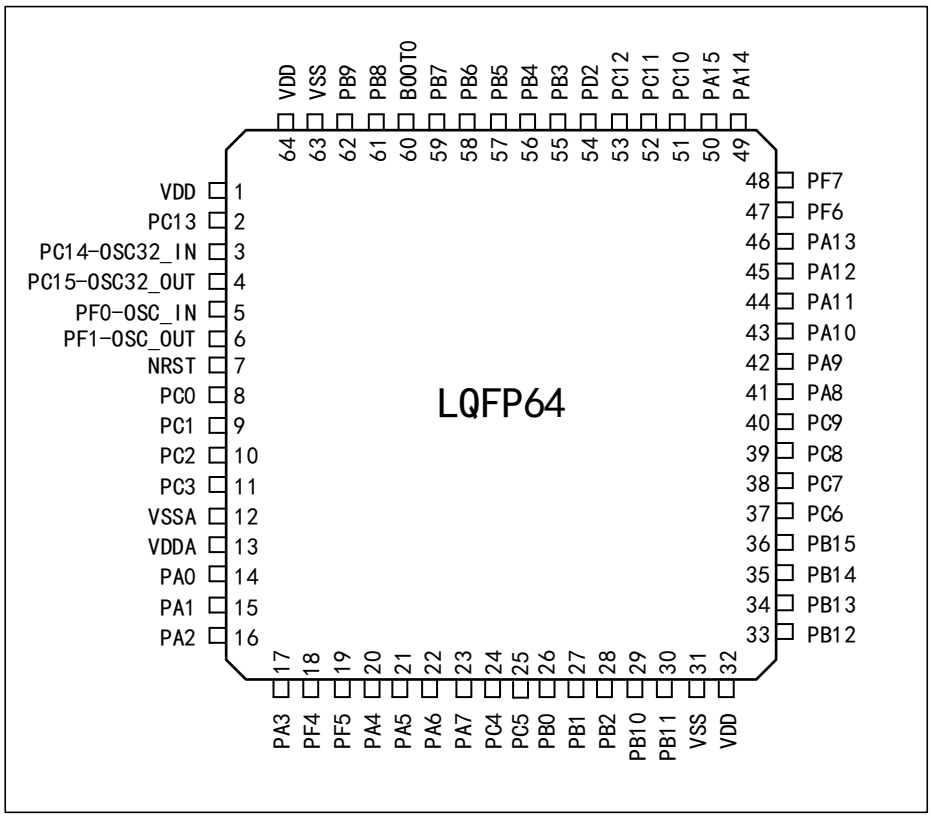


Figure 2 Distribution Diagram of APM32E030x8 Series LQFP48 Pins

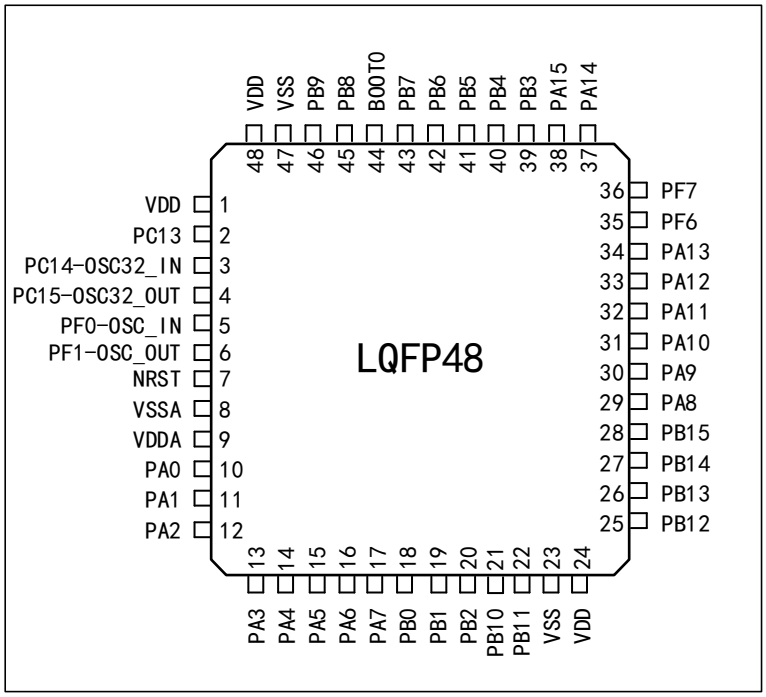


Figure 3 Distribution Diagram of APM32E030x8 Series LQFP32 Pins

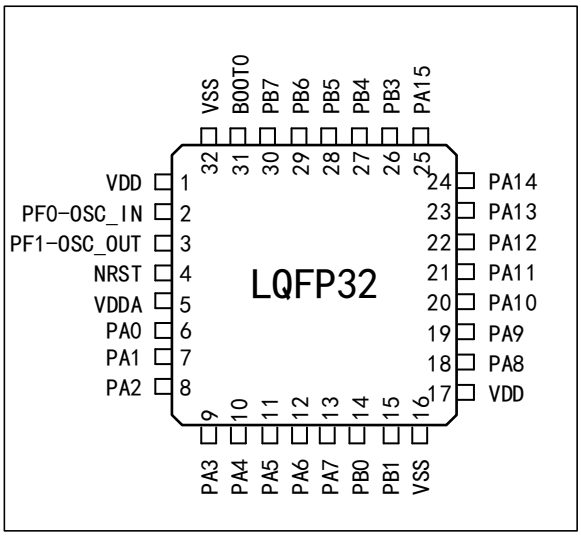


Figure 4 Distribution Diagram of APM32E030x8 Series QFN48 Pins

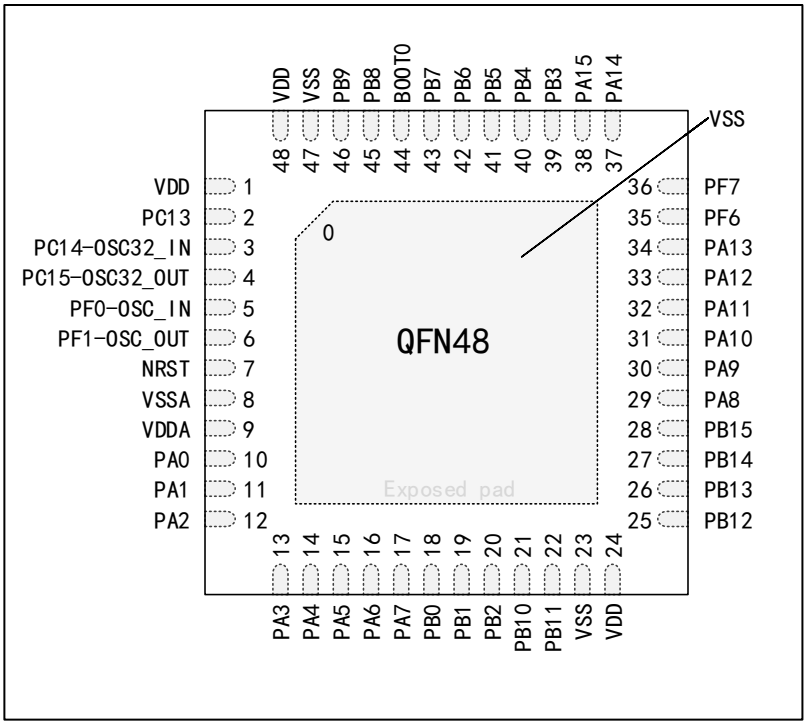


Figure 5 Distribution Diagram of APM32E030x8 Series QFN32 Pins

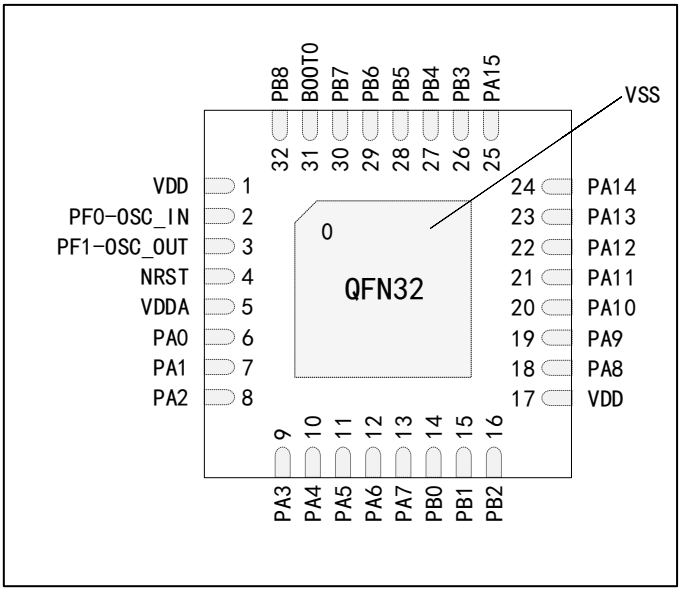


Figure 6 Distribution Diagram of APM32E030x8 Series QFN28 Pins

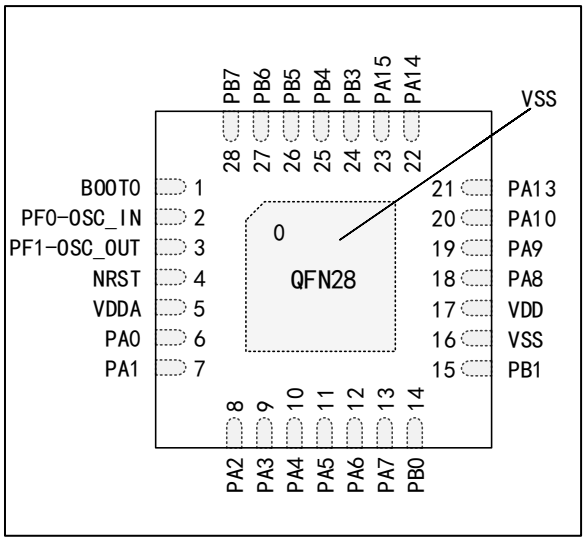
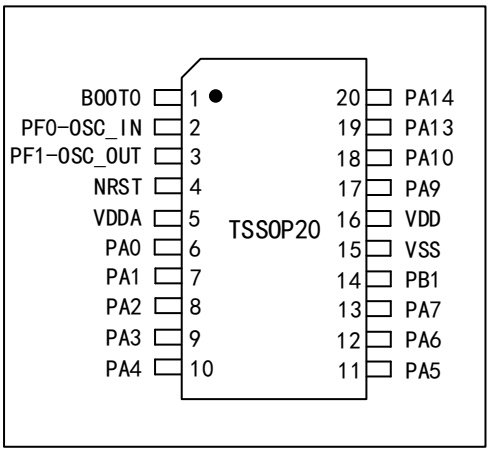


Figure 7 Distribution Diagram of APM32E030x8 Series TSSOP20 Pins



3.2 Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type	P	Power pin
	I	Only input pin
	I/O	I/O pin
I/O structure	5T	FT I/O
	5Tf	I/O, FM+ function with 5 V tolerance
	STDA	3.3V standard I/O, directly connected to ADC
	STD	3.3V standard I/O
	B	Dedicated Boot0 pin

Name		Abbreviation	Definition
		RST	Bidirectional reset pin with built-in pull-up resistor
Notes		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Default multiplexing function	Function directly selected/enabled through peripheral register	
	Additional function	Select this function through AFIO remapping register	

Table 3 Description of APM32E030x8 by Pin Number

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	TSSOP20	QFN28	QFN32	LQFP32	LQFP48 QFP48	LQFP64
V_{DD}	P	-	Chip complementary power supply		-	-	-	-	1	1
PC13[1]	I/O	STD	-	RTC_TS, RTC_OUT, WKUP2	-	-	-	-	2	2
PC14-OSC32_IN (PC14) [1]	I/O	STD	-	OSC32_IN	-	-	-	-	3	3
PC15-OSC32_OUT (PC15) [1]	I/O	STD	-	OSC32-OUT	-	-	-	-	4	4
PF0-OSC_IN (PF0)	I/O	5T	-	OCS_IN	2	2	2	2	5	5
PF1-OSC_OUT (PF1)	I/O	5T		OSC_OUT	3	3	3	3	6	6
NRST	I/O	RST	Chip reset input/internal reset output (active low)		4	4	4	4	7	7
PC0	I/O	STDA	EVENTOUT	ADC_IN10	-	-	-	-	-	8
PC1	I/O	STDA	EVENTOUT	ADC_IN11	-	-	-	-	-	9
PC2	I/O	STDA	EVENTOUT	ADC_IN12	-	-	-	-	-	10
PC3	I/O	STDA	EVENTOUT	ADC_IN13	-	-	-	-	-	11
V_{SSA}	P	-	Analog ground		-	-	0	-	8	12
V_{DDA}	P	-	Analog power supply		5	5	5	5	9	13

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	TSSOP20	QFN28	QFN32	LQFP32	LQFP48 QFP48	LQFP64
PA0	I/O	STDA	USART2_CTS	ADC_IN0, RTC_TAMP2, WKUP1	6	6	6	6	10	14
PA1	I/O	STDA	UASRT2_RTS, EVENTOUT	ADC_IN1	7	7	7	7	11	15
PA2	I/O	STDA	USART2_TX, TMR15_CH1	ADC_IN2	8	8	8	8	12	16
PA3	I/O	STDA	USART2_RX, TMR15_CH2	ADC_IN3	9	9	9	9	13	17
PF4	I/O	5T	EVENTOUT	-	-			-	-	18
PF5	I/O	5T	EVENTOUT	-	-			-	-	19
PA4	I/O	STDA	SPI1_NSS, USART2_CK, TMR14_CH1	ADC_IN4	10	10	10	10	14	20
PA5	I/O	STDA	SPI1_SCK	ADC_IN5	11	11	11	11	15	21
PA6	I/O	STDA	SPI1_MISO, TMR3_CH1, TMR1_BKIN, TMR16_CH1, EVENTOUT	ADC_IN6	12	12	12	12	16	22
PA7	I/O	STDA	SPI1_MOSI, TMR3_CH2, TMR14_CH1, TRM1_CH1N,	ADC_IN7	13	13	13	13	17	23

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	TSSOP20	QFN28	QFN32	LQFP32	LQFP48 QFP48	LQFP64
			TMR17_CH1, EVENTOUT							
PC4	I/O	STDA	EVENTOUT	ADC_IN14	-	-	-	-	-	24
PC5	I/O	STDA	-	ADC_IN15	-	-	-	-	-	25
PB0	I/O	STDA	TMR3_CH3, TMR1_CH2N, EVENTOUT	ADC_IN8	-	14	14	14	18	26
PB1	I/O	STDA	TMR3_CH4, TMR14_CH1, TMR1_CH3N	ADC_IN9	14	15	15	15	19	27
PB2	I/O	5T	-	-	-	-	16	-	20	28
PB10	I/O	5T	I2C2_SCL	-	-	-	-	-	21	29
PB11	I/O	5T	I2C2_SDA, EVENTOUT	-	-	-	-	-	22	30
V_{SS}	P	-	Digital ground		-	16	0	16	23	31
V_{DD}	P	-	Digital power supply		16	17	17	17	24	32
PB12	I/O	5T	SPI2_NSS, TMR1_BKIN, EVENTOUT	-	-	-	-	-	25	33
PB13	I/O	5T	SPI2_SCK, TMR1_CH1N	-	-	-	-	-	26	34
PB14	I/O	5T	SPI2_MISO, TMR1_CH2N, TMR15_CH1	-	-	-	-	-	27	35

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	TSSOP20	QFN28	QFN32	LQFP32	LQFP48 QFP48	LQFP64
PB15	I/O	5T	SPI2_MOSI, TMR1_CH3N, TMR15_CH1N, TMR15_CH2	RTC_REFIN	-	-	-	-	28	36
PC6	I/O	5T	TMR3_CH1	-	-	-	-	-	-	37
PC7	I/O	5T	TMR3_CH2	-	-	-	-	-	-	38
PC8	I/O	5T	TMR3_CH3	-	-	-	-	-	-	39
PC9	I/O	5T	TMR3_CH4	-	-	-	-	-	-	40
PA8	I/O	5T	USART1_CK, TMR1_CH1, EVENTOUT, MCO	-	-	18	18	18	29	41
PA9	I/O	5T	USART1_TX, TMR1_CH2, TMR15_BKIN	-	17	19	19	19	30	42
PA10	I/O	5T	USART1_RX, TMR1_CH3, TMR17_BKIN	-	18	20	20	20	31	43
PA11	I/O	5T	USART1_CTS, TMR1_CH4, EVENTOUT	-	-	-	21	21	32	44
PA12	I/O	5T	USART1_RTS, TMR1_ETR, EVENTOUT	-	-	-	22	22	33	45

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	TSSOP20	QFN28	QFN32	LQFP32	LQFP48 QFP48	LQFP64
PA13 (SWDIO)[2]	I/O	5T	IR_OUT, SWDIO	-	19	21	23	23	34	46
PF6	I/O	5T	I2C2_SCL	-	-	-	-	-	35	47
PF7	I/O	5T	I2C2_SDA	-	-	-	-	-	36	48
PA14 (SWCLK) [2]	I/O	5T	USART2_TX, SWCLK	-	20	22	24	24	37	49
PA15	I/O	5T	SPI1_NSS, USART2_RX, EVENTOUT	-	-	23	25	25	38	50
PC10	I/O	5T	-	-	-	-	-	-	-	51
PC11	I/O	5T	-	-	-	-	-	-	-	52
PC12	I/O	5T	-	-	-	-	-	-	-	53
PD2	I/O	5T	TMR3_ETR	-	-	-	-	-	-	54
PB3	I/O	5T	SPI1_SCK, EVENTOUT	-	-	24	26	26	39	55
PB4	I/O	5T	SPI1_MISO, TMR3_CH1, EVENTOUT	-	-	25	27	27	40	56
PB5	I/O	5T	SPI1_MOSI, I2C1_SMBA, TMR16_BKIN, TMR3_CH2	-	-	26	28	28	41	57

Name (Function after reset)	Type	Structure	Multiplexing function	Additional function	TSSOP20	QFN28	QFN32	LQFP32	LQFP48 QFP48	LQFP64
PB6	I/O	5T	I2C1_SCL, USART1_TX, TMR16_CH1N	-	-	27	29	29	42	58
PB7	I/O	5T	I2C1_SDA, USART1_RX, TMR17_CH1N	-	-	28	30	30	43	59
BOOT0	I	B	Memory startup selection		1	1	31	31	44	60
PB8	I/O	5Tf	I2C1_SCL, TMR16_CH1	-	-	-	32	-	45	61
PB9	I/O	5Tf	I2C1_SDA, IR_OUT, TMR17_CH1, EVENTOUT	-	-	-	-	-	46	62
V_{SS}	P	-	Digital ground		15	0	0	32	47/0	63
V_{DD}	P	-	Digital power supply		16	-	1	1	48	64

Note:

(1) PC13, PC14, and PC15 pins supply power through a power switch that can only absorb a limited amount of current (3mA). Therefore, these three pins have the following limitations as the GPIO output pin function: only one pin can be used as the output at the same time, as the output pin can only work in 2MHz mode, the maximum drive load is 30pF, the turnover frequency does not exceed 2MHz, and can not be used as a current source (such as driving LED).

(2) Upon reset, these pins are configured as SWDIO and SWCLK multiplexing functions, and the internal pull-up of SWDIO pin and the internal pull-down of SWCLK pin are activated.

3.3 GPIO Multiplexing Function Configuration

Table 4 GPIOA Multiplexing Function Configuration

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PA0	-	USART2_CTS	-	-	-	-	-
PA1	EVENTOUT	USART2_RTS	-	-	-	-	-
PA2	TMR15_CH1	USART2_TX	-	-	-	-	-
PA3	TMR15_CH2	USART2_RX	-	-	-	-	-
PA4	SPI1_NSS	USART2_CK	-	-	TMR14_CH1	-	-
PA5	SPI1_SCK	-	-	-	-	-	-
PA6	SPI1_MISO	TMR3_CH1	TMR1_BKIN	-	-	TMR16_CH1	EVENTOUT
PA7	SPI1_MOSI	TMR3_CH2	TMR1_CH1N	-	TMR14_CH1	TMR17_CH1	EVENTOUT
PA8	MCO	USART1_CK	TMR1_CH1	EVENTOUT	-	-	-
PA9	TMR15_BKIN	USART1_TX	TMR1_CH2	-	-	-	-
PA10	TMR17_BKIN	USART1_RX	TMR1_CH3	-	-	-	-
PA11	EVENTOUT	USART1_CTS	TMR1_CH4	-	-	-	-
PA12	EVENTOUT	USART1_RTS	TMR1_ETR	-	-	-	-
PA13	SWDIO	IR_OUT	-	-	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-
PA15	SPI1_NSS	USART2_RX	-	EVENTOUT	-	-	-

Table 5 GPIOB Multiplexing Function Configuration

Pin Name	AF0	AF1	AF2	AF3
PB0	EVENTOUT	TRM3_CH3	TMR1_CH2N	-
PB1	TMR14_CH1	TMR3_CH4	TMR1_CH3N	-
PB2	-	-	-	-
PB3	SPI1_SCK	EVENTOUT	-	-
PB4	SPI1_MISO	TMR3_CH1	EVENTOUT	-
PB5	SPI1_MOSI	TMR3_CH2	TMR16_BKIN	I2C1_SMBA
PB6	USART1_TX	I2C1_SCL	TMR16_CH1N	-
PB7	USART1_RX	I2C1_SDA	TMR17_CH1N	-
PB8	-	I2C1_SCL	TMR16_CH1	-
PB9	IR_OUT	I2C1_SDA	TMR17_CH1	EVENTOUT
PB10	-	I2C2_SCL	-	-
PB11	EVENTOUT	I2C2_SDA	-	-
PB12	SPI2_NSS	EVENTOUT	TMR1_BKIN	-
PB13	SPI2_SCK	-	TMR1_CH1N	-
PB14	SPI2_MISO	TMR15_CH1	TMR1_CH2N	-

Pin Name	AF0	AF1	AF2	AF3
PB15	SPI2_MOSI	TMR15_CH2	TMR1_CH3N	TMR15_CH1N

Table 6 GPIOC Multiplexing Function Configuration

Pin Name	AF0	AF1
PC0	EVENTOUT	-
PC1	EVENTOUT	-
PC2	EVENTOUT	-
PC3	EVENTOUT	-
PC4	EVENTOUT	-
PC5	-	-
PC6	TMR3_CH1	-
PC7	TMR3_CH2	-
PC8	TMR3_CH3	-
PC9	TMR3_CH4	-
PC10	-	-
PC11	-	-
PC12	-	-
PC13	-	-
PC14	-	-
PC15	-	-

Table 7 GPIOD Multiplexing Function Configuration

Pin Name	AF0	AF1
PD2	TMR3_ETR	-

Table 8 GPIOF Multiplexing Function Configuration

Pin Name	AF0	AF1
PF0	-	-
PF1	-	-
PF4	EVENTOUT	-
PF5	EVENTOUT	-
PF6	I2C2_SCL	-
PF7	I2C2_SDA	-

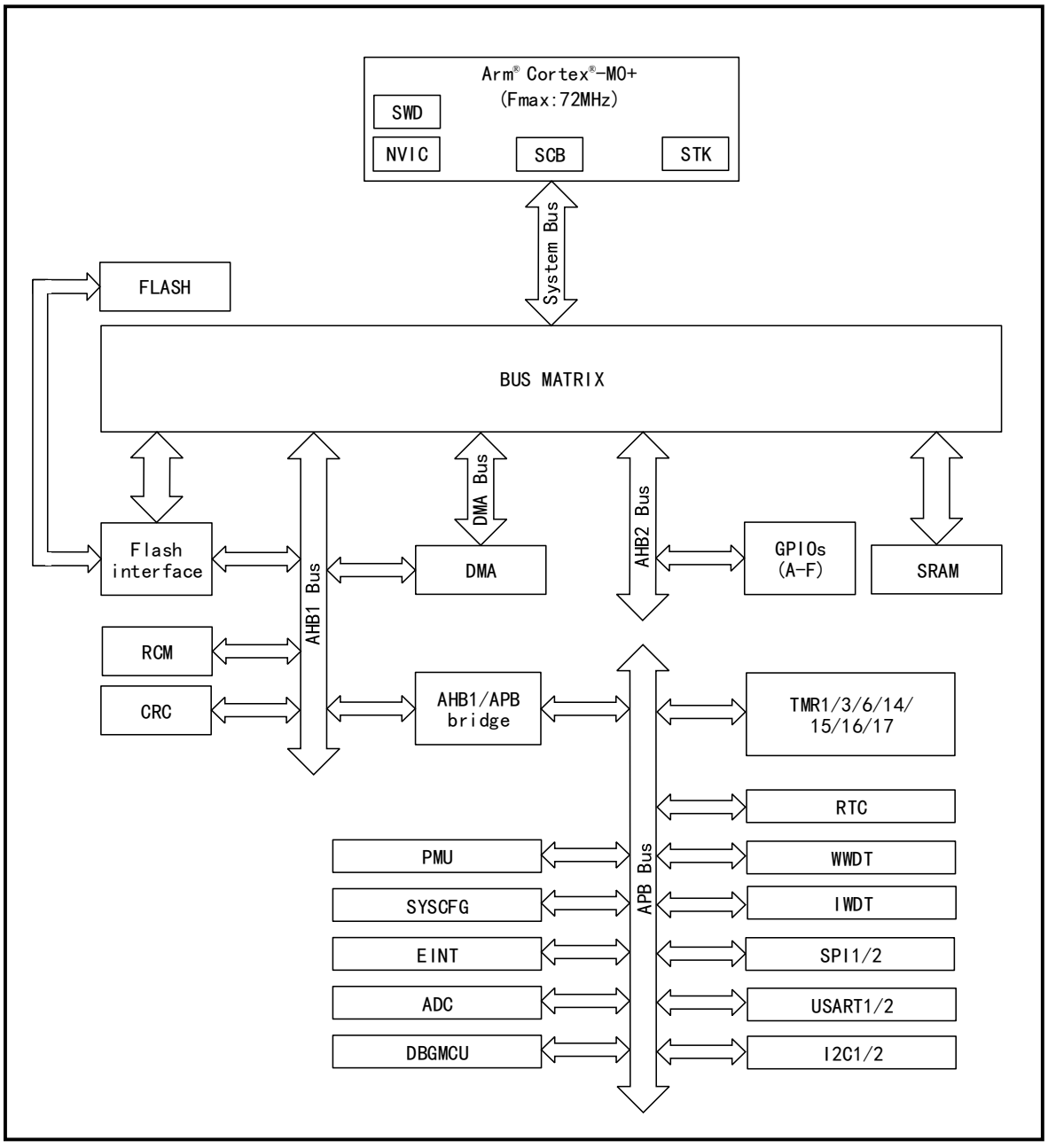
4 Function Description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32E030x8 series products; for information about the Arm® Cortex®-M0+ core, please refer to the *Arm® Cortex®-M0+ Technical Reference Manual*, which can be downloaded from Arm's website.

4.1 System architecture

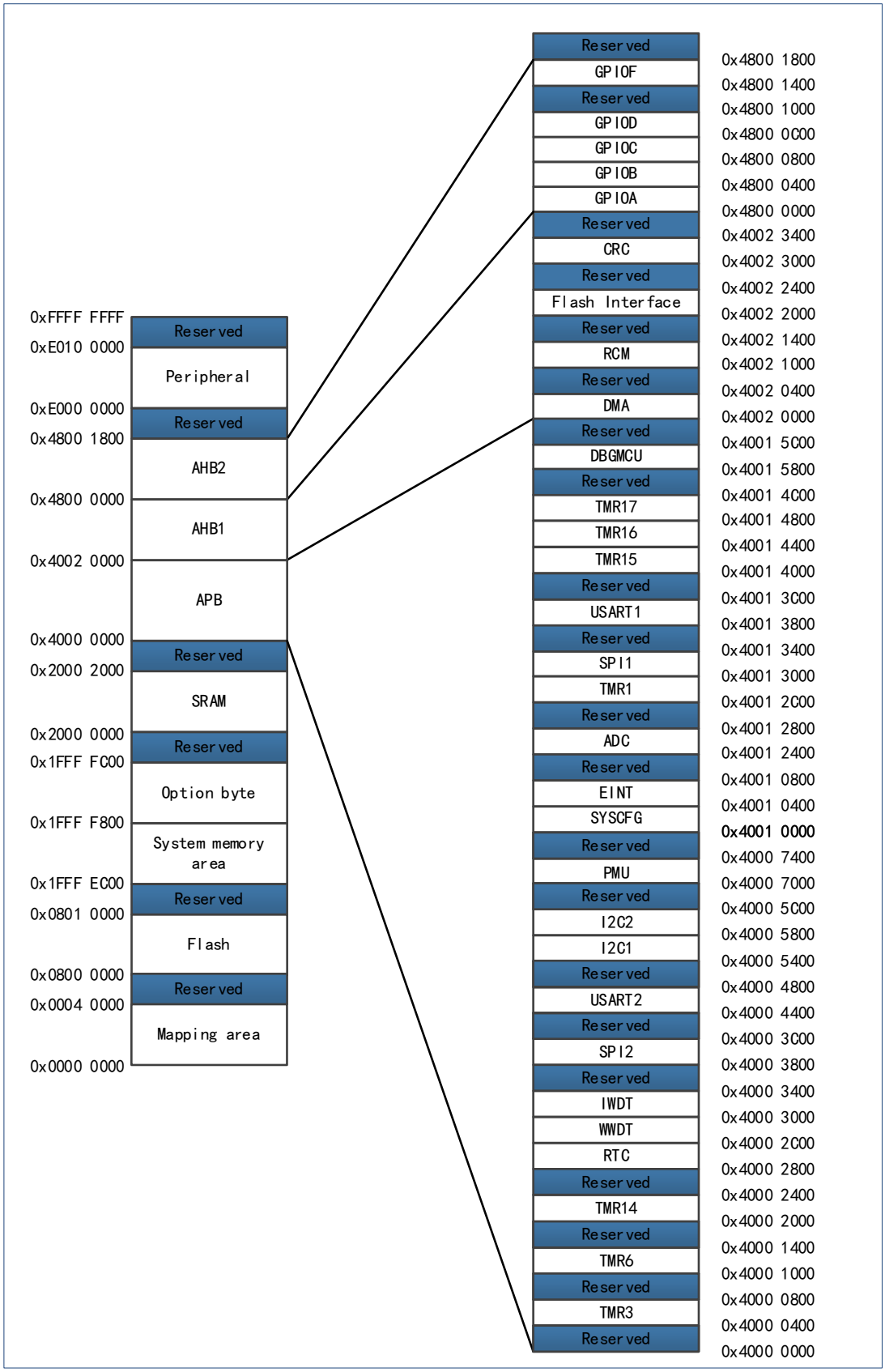
4.1.1 System block diagram

Figure 8 APM32E030x8 System Block Diagram



4.1.2 Address mapping

Figure 9 APM32E030x8 Series Address Mapping



4.1.3 Startup configuration

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from main memory
- Startup from BootLoader
- Startup from built-in SRAM

The user can use serial interface to reprogram the user Flash if starting up from BootLoader.

4.2 Core

The core of APM32E030x8 is Arm® Cortex®-M0+ with FPU computing unit. Based on this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all Arm tools and software.

4.3 Interrupt controller

4.3.1 Nested Vector Interrupt Controller (NVIC)

It embeds a nested vectored interrupt controller (NVIC) that can handle up to 32 maskable interrupt channels (not including 16 interrupt lines of Cortex®-M0+) and 4 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2 External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 32 edge detectors, and each detector includes edge detection circuit and interrupt/event request generation circuit; each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 55 GPIOs can be connected to 16 external interrupt lines.

4.4 On-chip memory

On-chip memory includes main memory area, SRAM and information block; the information block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written into the program when leaving the factory and cannot be erased.

Table 9 On-chip Memory Area

Memory	Maximum capacity	Function
Main memory area	64 KB	Store user programs and data
SRAM	8 KB	CPU can access at 0 wait cycle (read/write)
System memory area	3KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information

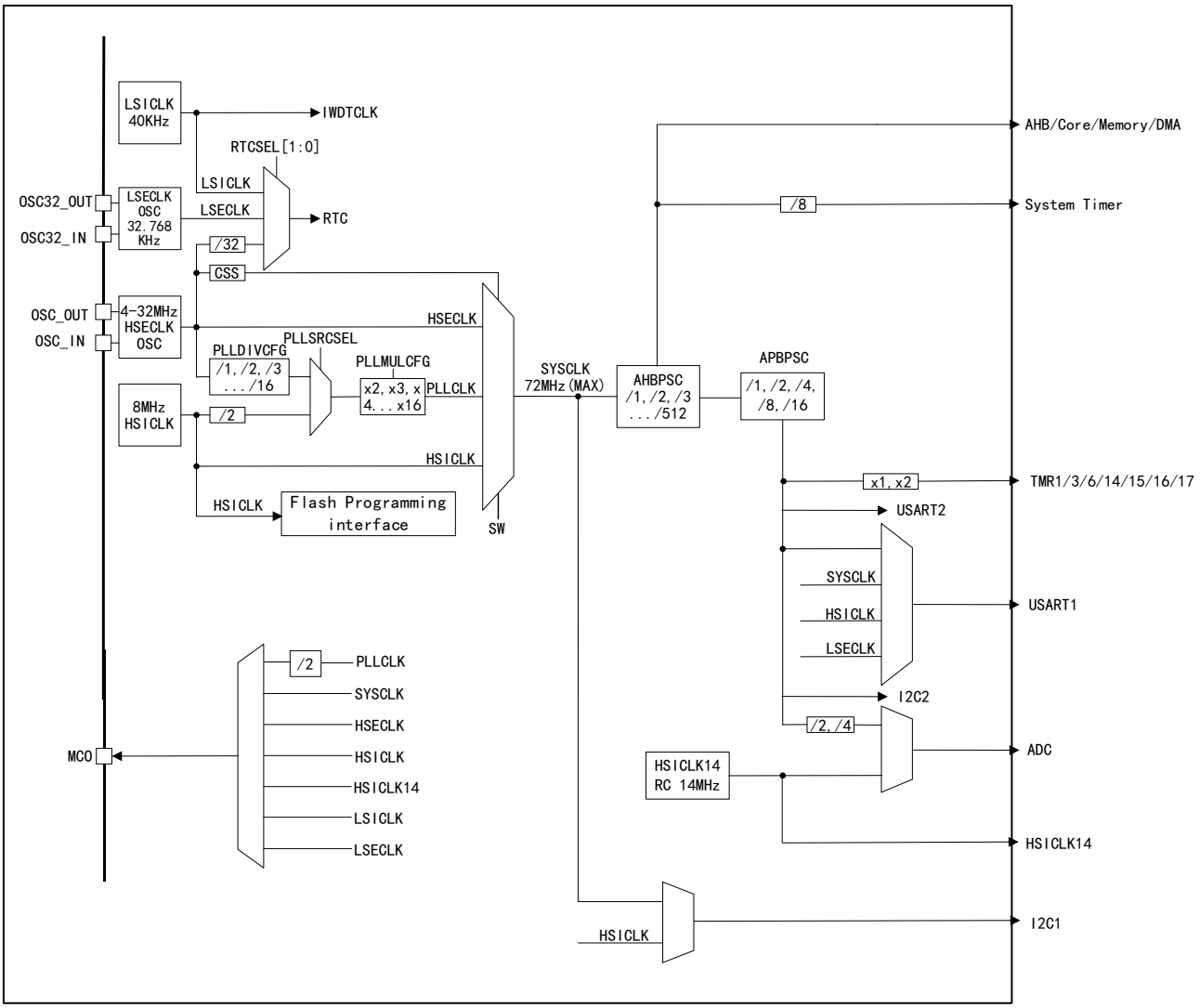
Memory	Maximum capacity	Function
Option byte	16Bytes	Configure main memory area read-write protection and MCU working mode

4.5 Clock

4.5.1 Clock tree

Clock tree of APM32E030x8 is shown in the figure below:

Figure 10 APM32E030x8 Clock Tree



4.5.2 Clock source

Clock source is divided into high-speed clock and low-speed clock according to the speed; the high-speed clock includes HSICLK and HSECLK, and the low-speed clock includes LSECLK and LSICLK; It is divided into internal clock and external clock according to in-chip/out-chip. The internal clock has HSICLK and LSICLK, and the external clock has HSECLK and LSECLK, among which the calibration accuracy of HSICLK is up to ±1% at the factory. HSICLK14 is a clock source dedicated to the ADC.

4.5.3 System clock

HSICLK, PLLCLK and HSECLK can be selected as system clock; the clock source of PLLCLK can be HSICLK or HSECLK; the required system clock can be obtained by configuring PLL clock multiplier factor and frequency division factor.

When the product is reset and started, HSICLK is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock. When HSECLK failure is detected, the system will automatically switch to the HSICLK, and if an interrupt is enabled, the software can receive the related interrupt.

4.5.4 Bus clock

AHB, APB buses are built in. The clock source of AHB is SYSCLK, and the clock source of APB is HCLK frequency division; the required clock can be obtained by configuring the frequency division factor. The maximum frequency of AHB and APB is 168MHz.

4.6 Power and power management

4.6.1 Power supply scheme

Table 10 Power Supply Scheme

Name	Voltage range	Description
V_{DD}/V_{SS}	2.0～3.6V	I/O (see pin distribution diagram for specific IO) and internal voltage regulator are powered through V_{DD} pin.
V_{DDA}/V_{SSA}	2.0～3.6V	Supply power for ADC, DAC, reset module, RC oscillator and PLL analog part; when ADC or DAC is used, V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.

Note: See Figure 11 (Power Scheme) for more information on how to connect the power pins.

4.6.2 Voltage regulator

Table 11 Regulator Operating Mode

Name	Description
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode; when the voltage regulator has high-impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3 Power supply voltage monitor

Power-on reset (POR), power-down reset (PDR) are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even if the external reset circuit is used, the system will remain reset.

4.7 Low-power mode

APM32E030x8 supports three low-power modes, namely, sleep mode, stop mode and standby mode, and there are differences in power, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual application requirements.

Table 12 Low-power Mode

Mode	Description
Sleep mode	The core stops working, all peripherals are working, and it can be woken up through interrupts/events
Stop mode	Under the condition that SRAM and register data are not lost, the lowest power consumption can be achieved in stop mode; The clock of the internal 1.2V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be disabled, and the voltage regulator can be configured in normal mode or low-power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, RTC and USB_OTG.
Standby mode	The power consumption in this mode is the lowest; Internal voltage regulator is turned off, all 1.2V power supply modules are powered down, HSECLK crystal resonator, and HSICLK clocks are disabled, SRAM and register data disappear, RTC area and backup register contents remain, and the standby circuit still works; The external reset signal on NRST, IWDT reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode.

Note: In down or standby mode, RTC, IWDT and corresponding clocks still work properly.

4.8 DMA

A built-in DMA supports five DMA channels, each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI, USART, I2C, TMRx. Four levels of DMA channel priority can be configured, and data transmission of "Memory → Memory, Memory → Peripheral, Peripheral → Memory" can be supported (memory includes Flash and SRAM).

4.9 GPIO

GPIO can be configured as general input mode, general output mode, multiplexing function mode and analog mode. The input mode can be configured as floating input, pull-up input and pull-down input; the output mode can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; and the analog mode can be used for analog peripherals; the enable and disable pull-up/pull-down resistor can be configured; the speed of Low speed, medium speed, high speed can be configured; the higher the speed is, the greater the power and the noise will be.

4.10 Communication peripherals

4.10.1 USART

Up to 2 universal synchronous/asynchronous transmitter receivers are built in the chip. The USART interfaces can communicate at a rate of 6Mbit/s. All USART interfaces can configure baud rate, parity check bit, stop bit, and data bit length; they all can support DMA. USART function differences are shown in the table below:

Table 13 USART/UART Function Differences

USART mode/function	USART1	USART2
Hardware flow control of modem	√	√
Multiprocessor communication	√	√
Synchronization mode	√	√
Receiver timeout interrupt	√	-
Auto baud rate detection (supported mode)	2	-
Single wire half duplex mode	√	√
Support DMA function	√	√

Note: √ = support.

4.10.2 I2C

I2C1/2 all can work in multiple-master or slave modes, support 7-bit or 10-bit addressing, and support dual-slave addressing supports standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s); In addition, the I2C1 has built-in programmable analog and digital noise filters and supports ultra-fast mode (up to 1Mbit/s); They can operate using DMA and support SMBus version 2.0 /PMBus1.1 buses. hardware CRC generator/checker are built in; they can operate with DMA and support SMBus 2.0 version/ PMBus.

Table 14 APM32E030x8 I2C Function

I2C function	I2C1	I2C2(2)
7-bit addressing mode	√ (1)	√
10-bit addressing mode	√	√
Standard mode (up to 100kbit/s)	√	√
Fast mode (up to 400kbit/s)	√	√
Ultra-fast mode (up to 1Mbit/s), I/O port supports 20mA output current drive	√	-
Independent clock	√	-
SM bus	√	-

Note:

(1) √ = support

(2) Available only on APM32E030x8 chip.

4.10.3 SPI

2 built-in SPI, support full-duplex and half-duplex communication in master mode and slave mode, can use DMA controller, and can configure 4~16 bits per frame, communicate at a rate of up to 18Mbit/s.

Table 15 APM32E030x8 SPI Function

SPI function	SPI	SPI2(2)
Calculation of hardware cyclic redundancy check	√(1)	√
Receive/Send first in first out (FIFO)	√	√
NSS pulse mode	√	√
TI mode	√	√

Note:

(1) √ = supported.

(2) Available only on APM32F030x8 chip.

4.11 Analog peripherals

4.11.1 ADC

A built-in ADC with 12-bit accuracy, up to 16 external channels and 2 internal channels. The internal channels measure the temperature sensor voltage, reference voltage respectively. A/D conversion mode of each channel has single, continuous, scan or intermittent modes, ADC conversion results can be left aligned or right aligned and stored in 16-bit data register; they support analog watchdog, and DMA.

4.11.1.1 Temperature sensor

1 temperature sensor (TSensor) is built in, which is internally connected with ADC_IN16 channel. The voltage generated by the sensor changes linearly with temperature and the converted voltage value can be obtained by ADC and converted into temperature.

Table 16 Calibration Value of Tsensor Voltage

Calibration Value Name	Description	Memory Address
V_{sensor_CAL1}	Tsensor ADC raw data acquied at V_{DDA}=3.3V(± 10mV) under 30℃(±5℃)	0x1FFF F7B8 - 0x1FFF F7B9

4.11.1.2 Internal reference voltage

Built-in reference voltage V_{REFINT}, internally connected to ADC_IN17 channel; V_{REFINT} can be obtained through ADC; V_{REFINT} provides stable voltage output for ADC.

Table 17 Calibration Value of Internal Reference Voltage

Calibration Value Name	Description	Memory Address
V_{REFINT_CAL}	Original data collected at V_{DDA}=3.3V(±10mV) under 30℃ (±5℃)	0x1FFF F7BA - 0x1FFF F7BB

4.12 Timer

A built-in 16-bit advanced timers (TMR1), 5 16-bit general-purpose timers (TMR3/14/15/16/17), 1 16-bit basic timers (TMR6), 1 independent watchdog timer, 1 window watchdog timer and 1 system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral of the core with automatic reloading function. When the counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

Table 18 Function Comparison between Advanced/General-purpose/Basic and System Tick Timers

Timer type	**System tick timer**	**Basic timer**	**General-purpose timer**				**Advanced timer**
Timer name	Sys Tick Timer	TMR6	TMR3	TMR14	TMR15	TMR16/17	TMR1
Counter resolution	24 bits	16 bits	16 bits				16 bits
Counter type	Down	Up	Up, down, up/down	Up			Up, down, up/down
Prescaler factor	-	Any integer between 1 and 65536	Any integer between 1 and 65536				Any integer between 1 and 65536
General DMA request	-	OK	OK	Not OK	OK		OK
Capture/ Comparison channel	-	-	4	1	2	1	4
Complementary outputs	-	No	No		Yes		Yes
Pin characteristics	-	-	1 external trigger signal input pin, 4 channels (non-complementary	1 channel (non-complementary channels) pin	1 brake input signal pin, 1 pair of complementary	1 brake input signal pin, 1 pair of complementary	A total of 9 pins:1 external trigger signal input pin, 1 brake input signal pin,

Timer type	System tick timer	Basic timer	General-purpose timer				Advanced timer
			channels) pins		channel pins, 1 channel (non-complementary channel) pin	channel pins	3 pairs of complementary channel pins, 1 channel (non-complementary channel) pin
Function Instruction	Special for real-time operating system Automatic reloading function supported When the counter is 0, it can generate a maskable system interrupt Can program the clock source	Can be used as a 16-bit general-purpose timebase counter.	There are 4 independent channels, each for input capture/output comparison, PWM or single pulse mode output. Has a separate DMA request.	Single channel, PWM or single pulse mode output function for input capture/output comparison.	It has complementary output function with dead zone generation and independent DMA request generation. These three timers can work together, and TMR15 operates with TMR1 through link function, which can realize synchronization or event link function. TMR15 has two independent channels, while TMR16 and TMR17 are synchronized. TMR15 can be synchronized with TMR16 and TMR17.		It has complementary PWM output with dead band insertion When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, the timer can be frozen, and PWM output is disabled. Synchronization or event chaining function provided.

Table 19 Function Comparison between IWDT and WWDT

Name	Counter resolution	Counter type	Prescaler factor	Function description
Independent watchdog	12 bits	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator of 40KHz, which is independent of the master clock, so it can run in stop and standby modes.

Name	Counter resolution	Counter type	Prescaler factor	Function description
				The whole system can be reset in case of problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. Timers in debug mode can be frozen.
Window watchdog	7 bits	Down	-	Can be set for free running. The whole system can be reset in case of problems. Driven by the master clock, it has early interrupt warning function; Timers in debug mode can be frozen.

4.13 RTC

1 RTC is built in, and there are LSECLK signal input pins (OS32_IN and OS32_OUT) and 1 TAMP input signal detection pins (TAMP); the clock source can select external 32.768kHz crystal oscillator, resonator or oscillator, LSICLK and HSECLK/32.

Users can dynamically adjust the RTC clock pulse from 1 to 32767. By adjusting the RTC clock pulse to synchronize the RTC and master clock, it compensates for the accuracy of the crystal oscillator, and its digital calibration circuit has a resolution of 1ppm. The RTC has two programmable filter tamper-proof detection pins that wake up the MCU in down and standby mode when this pin detects a tampering event. In addition to this, RTC has a time stamp function that can be used to save calendar content. The time stamp function of the RTC can be triggered by events on the pin or tampering events. Upon detection of a time event rainbow, the MCU can wake up from both down and standby modes. Its reference clock detection may improve the accuracy of the calendar by using a more accurate second source clock (50 or 60Hz).

4.14 CRC

1 CRC (cyclic redundancy check) computing unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

5 Electrical Characteristics

5.1 Test conditions of electrical characteristics

5.1.1 Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

5.1.2 Typical value

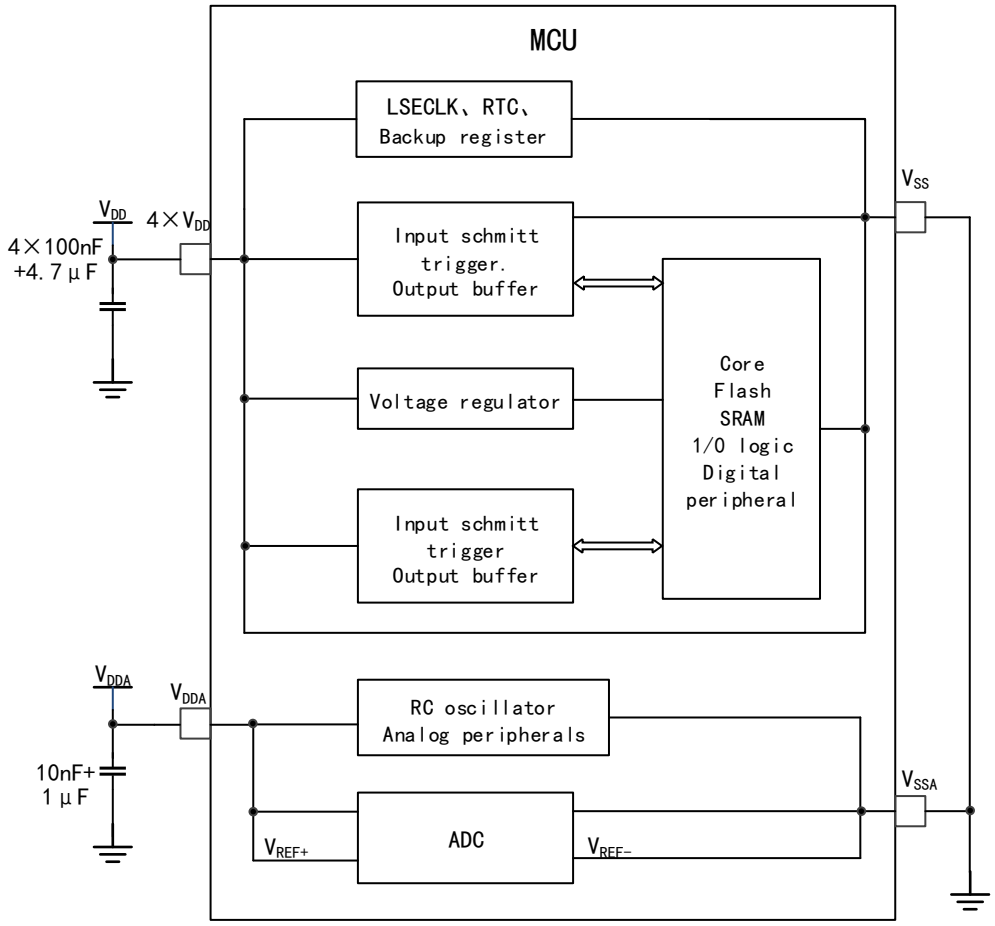
Unless otherwise specified, typical data are measured based on T_A=25℃, V_{DD}=V_{DDA}=3.3V. These data are only used for design guidance.

5.1.3 Typical curve

Unless otherwise specified, typical curves will only be used for design guidance and will not be tested.

5.1.4 Power supply scheme

Figure 11 Power Supply Scheme



5.1.5 Load capacitance

Figure 12 Load conditions when measuring pin parameters

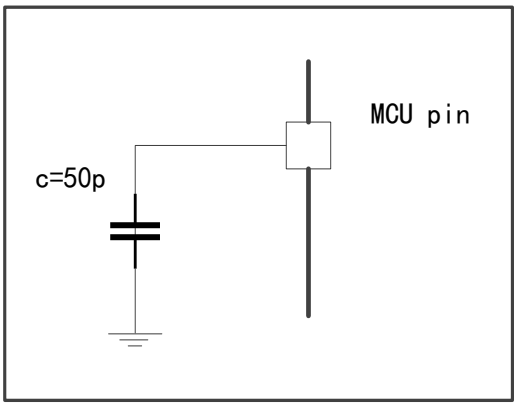


Figure 13 Pin Input Voltage Measurement Scheme

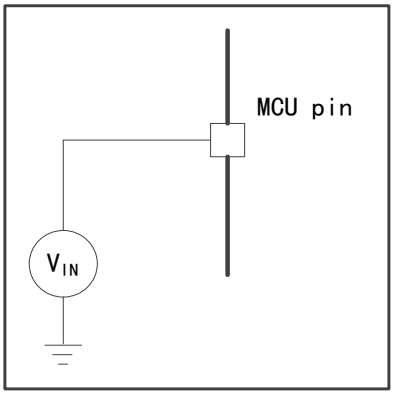
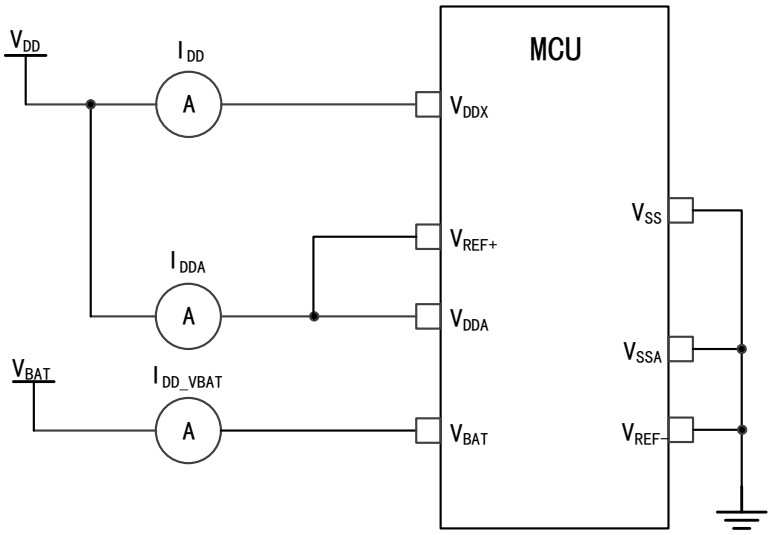


Figure 14 Power Consumption Measurement Scheme



5.2 Test under general operating conditions

Table 20 General Operating Conditions

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	72	MHz
f_{PCLK}	Internal APB clock frequency	-	-	72	
V_{DD}	Main power supply voltage	-	2	3.6	V
V_{DDA}	Analog power supply voltage	V_{DDA} must not be smaller than V_{DD}	2.4	3.6	V

5.3 Absolute maximum ratings

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.3.1 Maximum temperature characteristics

Table 21 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-65 ~ +150	℃
T_J	Maximum junction temperature	125	℃

5.3.2 Maximum rated voltage characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 22 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD}-V_{SS}	External main supply voltage (V_{DD})	-0.3	4.0	V
V_{DDA}-V_{SSA}	External analog supply voltage（V_{DDA}）	-0.3	4.0	
V_{DD}-V_{DDA}	Allowable voltage difference of V_{DD}>V_{DDA}	-	0.4	
V_{IN}	Input voltage on 5T pins	V_{SS}-0.3	V_{DD} + 4.0	
	Boot0	0	V_{DD} + 4.0	
	Input voltage on any other pin	V_{SS}-0.3	V_{DD} + 0.3	
$\|\Delta V_{DDx}\|$	Voltage difference between different power supply pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Voltage difference between different grounding pins	-	50	

Note:

(1) Some power supply (V_{DD},V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to a power supply within an external limited range.

(2) If V_{IN} is within the maximum range, $I_{INJ(PIN)}$ will not exceed its limit. If V_{IN} exceeds the maximum value, the value of the $I_{INJ(PIN)}$ must be externally restricted to ensure that its maximum value is not exceeded. The forward injection current occurs when V_{IN} is greater than V_{DD}, and the reverse injection current occurs when V_{IN} is less than V_{SS}.

5.3.3 Maximum rated current characteristics

Table 23 Current Characteristics

Symbol	Description	Maximum value	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	-120	
$I_{VDD\ (PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$I_{VSS\ (PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	-100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$I_{INJ(PIN)}$ (3)	Injected current on 5T pins	-5/+0(4)	
	Injected current on TC and RST pin	±5	

Symbol	Description	Maximum value	Unit
	Injected current on TTa pins(5)	±5	
$\Sigma I_{INJ(PIN)}$(2)	Total injected current (sum of all I/O and control pins)(6)	±25	

Note:

(1) All power (VDD，VDDA) and ground (VSS，VSSA) pins must always be connected to a power supply within the external allowable range.

(2) If VIN does not exceed the maximum value, IINJ(PIN) will not exceed its limit. If VIN exceeds the maximum value, IINJ(PIN) must be externally limited to not exceed its maximum value. When VIN > VDD, there is a forward injection current; when VIN < VSS, there is a reverse injection current.

(3) Reverse injection current can interfere with the analog performance of the ADC.

(4) When several I/O ports have injection current at the same Time, the maximum value of ΣIINJ(PIN) is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. These results are based on the calculation of the maximum value of ΣIINJ(PIN) on the four I/O port pins of the device.

(5) On these I/Os, a positive injection is induced by VIN > VDDA. Negative injection disturbs the analog performance of the device.

(6) When several inputs are submitted to a current injection, the maximum ΣIINJ(PIN) is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3.4 Electro-static discharge (ESD)

Table 24 ESD Absolute Maximum Ratings

Symbol	Parameter	Conditions	Range	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (manikin)	T_A=+25℃	±4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A=+25℃	±1000	V

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.3.5 Static latch-up (LU)

Table 25 Static Latch-up

Symbol	Parameter	Conditions	Type
LU	Class of static latch-up	T_A= +25 ℃/+105℃, Comply with EIA/JESD78E	Class II A

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.4 Memory

5.4.1 Flash characteristics

Table 26 Flash Memory Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{prog}	16-bit programming time	T_A=-40~85°C V_{DD}=2.0~3.6V	59	60	61	μs

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{ERASE}	Page (1Kbytes) erase time	T_A=-40~85°C V_{DD}=2.0~3.6V	3.2	-	4	ms
t_{ME}	Whole erase time	T_A=-40~85°C V_{DD}=2.0~3.6V	8	-	10	ms
V_{prog}	Programming voltage	T_A=-40~85°C	1.84	-	3.6	V
t_{RET}	Data saving time	T_A=55℃	20	-	-	years
N_{RW}	Erase cycle	T_A=25°C	10K	-	-	cycles
-	0 Waiting period Maximum running time of the FLASH	-	30	40	48	MHz

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.5 Clock

5.5.1 Characteristics of external clock source

High-speed external clock generated by crystal resonator(HSECLK)

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 27 HSECLK4~32MHz Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistance	-	-	200	-	kΩ
$I_{DD(HSECLK)}$	HSECLK current consumption	V_{DD}=3.3V, Single side load capacitance of crystal oscillator pinCL=20pF@8MHz	-	0.5	-	mA
$t_{SU(HSECLK)}$	Start-up Time	V_{DD} is stable	-	1	2	ms

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Low-speed external clock generated by crystal resonator(LSECLK)

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 28 LSECLK Oscillator Characteristics (f_{LSECLK} =32.768KHz)(1)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	-	32.768	-	KHz

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$I_{DD(LSECLK)}$	LSECLK current consumption	-	-	1.2	1.5	μA
$t_{SU(LSECLK)}$(2)	Start-up Time	V_{DD} is stable	-	0.2	0.5	s

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) $t_{SU(LSECLK)}$ is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured by using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

5.5.2 Characteristics of internal clock source

High-speed internal (HSICLK) RC oscillator

Table 29 HSICLK Oscillator Characteristics

Symbol	Parameter	Conditions		Minimum value	Typical value	Maximum value	Unit
f_{HSICLK}	Frequency	-		-	8	-	MHz
$A_{CC(HSICLK)}$	Accuracy of HSICLK oscillator	Factory calibration	V_{DD}=3.3V，T_A=25℃(1)	-1	-	1	%
			V_{DD}=2-3.6V，T_A=-40~85℃	-1.5	-	1.5	%
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-		-	75	94	μA
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=3.3V，T_A=-40~85℃		-	0.3	1.1	μs

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Table 30 HSICLK14 Oscillator Characteristics

Symbol	Parameter	Conditions		Minimum value	Typical value	Maximum value	Unit
$f_{HSICLK14}$	Frequency	-		-	14	-	MHz
$A_{CC(HSICLK14)}$	Accuracy of HSICLK14 oscillator	Factory calibration	-1	-	1	1	%
			-5	-	5	1.5	%
$I_{DDA(HSICLK14)}$	Power consumption of HSICLK14 oscillator	-		73	90	114	μA
$t_{SU(HSICLK14)}$	Startup time of	V_{DD}=3.3V，T_A=-40~85℃		0.5	0.7	1	μs

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
	HSICLK14 oscillator					

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Low-speed internal (LSICLK) RC oscillator

Table 31 LSICLK Oscillator Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{LSICLK}	Frequency (V_{DD}=2-3.6V, T_A =-40~85℃)	30	35	50	KHz
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	-	0.4	0.64	μA
$t_{SU(LSICLK)}$	Startup time of LSICLK oscillator, (V_{DD}=3.3V，T_A=-40~85℃)	-	-	30	μs

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.5.3 PLL Characteristics

Table 32 PLL Characteristics

Symbol	Parameter	Value			Unit
		Minimum value	Typical value	Maximum value	
f_{PLL1_IN}	PLL input clock	1	8	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency multiplier output clock (V_{DD}=3.3V, T_A=-40~85℃)	16	-	72	MHz
t_{LOCK1}	PLL phase locking time	-	-	200	μs

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.6 Reset and power management

5.6.1 Test of Embedded Reset and Power Control Module Characteristics

Table 33 Embedded Reset and Power Control Module Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{POR/PDR}$(1)	Power-on/power-down reset threshold	Falling edge(2)	-	1.87	-	V
		Rising edge	-	1.92	-	V
$V_{PDRhyst}$(3)	PDR hysteresis	-	-	50.00	-	mV
$T_{RSTTEMPO}$(3)	Reset duration (3.3~3.6V)	-	1.6	4.44	5.68	ms
	Reset duration (2V)	-	8.4	12.86	16.8	

Note:

(1) PDR detector monitors V_{DD} and V_{DDA} (if enabled in option byte), POR detector monitors V_{DD} only.

(2) Product characteristics are guaranteed by design to the minimum $V_{POR/PDR}$ value.

(3) Guaranteed by design and not tested in production.

5.7 Power consumption

5.7.1 Power consumption test environment

（1） The values are measured by executing Dhrystone 2.1, with the Keil.V5 compilation environment and the L0 compilation optimization level.

（2） All I/O pins are in analog input mode and are connected to a static level at V_{DD} or V_{SS} (no load)

（3） Unless otherwise specified, all peripherals are disabled

（4） The relationship between Flash wait cycle setting and f_{HCLK}:

0~24MHz: 0 wait cycle

24~48MHz: 1 wait cycle

48~72MHz: 2 wait cycles

（5） When it is greater than 24MHz, the instruction prefetch function is enabled (Note: this bit must be set before clock setting and bus frequency division).

（6） When the peripheral is turned on: $f_{PCLK}=f_{HCLK}$.

5.7.2 Power consumption in running mode

Table 34 Power Consumption in Running Mode when the Program is Executed in Flash

Mode	Condition	f_{HCLK}	T_A=25℃，V_{DD}=3.3V				T_A=85℃，V_{DD}=3.6V			
			I_{DDA}(μA)		I_{DD}(mA)		I_{DDA}(μA)		I_{DD}(mA)	
			Typical value	Maximum value	Typical value	Maximum value	Typical value	Maximum value	Typical value	Maximum value
Running mode	HSECLK(1), enabling all peripherals	72MHz	226.8	231.3	6.39	6.52	245.3	249.9	6.47	6.61
		48MHz	178.2	182.2	5.25	5.35	193.1	196.8	5.28	5.32
		24MHz	135.5	138.9	4.08	4.14	148.9	152.4	4.17	4.20
		8MHz	123.6	126.9	1.93	1.94	137.0	140.5	2.01	2.02
	HSECLK(1), turn off all peripherals	72MHz	226.8	231.1	4.11	4.2	245.3	249.8	4.14	4.19
		48MHz	178.1	181.9	3.75	3.84	193	197	3.82	3.89
		24MHz	135.5	138.9	3.33	3.39	148.9	152.4	3.41	3.44
		8MHz	123.6	127.0	1.66	1.67	136.9	140.4	1.73	1.75
	HSICLK, enable all peripherals	64MHz	211.8	215.5	4.74	5.17	234	237.2	4.81	5.28
		48MHz	179.9	183.1	3.53	3.9	198.8	201.4	3.62	4.01
		24MHz	137.4	140.4	2.07	2.46	153.9	156.1	2.15	2.56
		8MHz	125.3	127.7	1.02	1.37	141.8	144	1.09	1.43
	HSICLK, turn off all peripherals	64MHz	211.9	215.6	2.65	3.12	234	237	2.73	3.22
		48MHz	179.8	183.3	2.07	2.42	198.8	201.7	2.15	2.51
		24MHz	137.2	140.1	1.32	1.72	153.8	156.2	1.39	1.79
		8MHz	125.2	127.8	0.75	1.1	141.6	143.7	0.82	1.16

Note: HSECLK external crystal oscillator is 8MHz, and when f_{HCLK}>8MHz, turn on PLL. Otherwise, turn off PLL.

Table 35 Power Consumption in Run Mode when the Program is Executed in SRAM

Mode	Condition	f_{HCLK}	T_A=25℃，V_{DD}=3.3V				T_A=85℃，V_{DD}=3.6V			
			I_{DDA}(μA)		I_{DD}(mA）		I_{DDA}(μA)		I_{DD}(mA)	
			Typical value	Maximum value	Typical value	Maximum value	Typical value	Maximum value	Typical value	Maximum value
Running mode	HSECLK(1), enabling all peripherals	72MHz	150.29	155.63	5.65	5.78	160.1	164.9	5.74	5.81
		48MHz	101.66	106.32	3.95	4.05	107.8	112	4	4.06
		24MHz	58.98	63.42	2.37	2.39	63.4	67.5	2.44	2.54
		8MHz	47.07	51.36	1.3	1.31	51.4	55.5	1.38	1.47
	HSECLK(1), turn off all peripherals	72MHz	150.32	155.93	3.45	3.57	159.7	164	3.56	3.67
		48MHz	101.62	106.17	2.57	2.63	107.6	112	2.63	2.7
		24MHz	59.04	63.27	1.66	1.68	63.4	67.2	1.74	1.83
		8MHz	47.1	51.2	1.06	1.07	51.5	55.9	1.14	1.23
	HSICLK, enable all peripherals	64MHz	211.5	214.4	3.01	3.11	234.1	237.3	3.04	3.08
		48MHz	179.4	182.0	2.1	2.14	198.9	201.4	2.16	2.19
		24MHz	136.9	139.0	1.19	1.22	154	156.2	1.27	1.28
		8MHz	124.9	127.4	0.57	0.58	141.7	144.2	0.63	0.64
	HSICLK, turn off all peripherals	64MHz	212.9	237.2	2.64	2.7	234	237	2.77	2.85
		48MHz	180.0	201.7	2.06	2.11	198.9	201.4	2.13	2.15
		24MHz	136.4	156.4	1.17	1.19	153.9	156.4	1.23	1.25
		8MHz	124.9	127.2	0.57	0.58	141.8	144.6	0.63	0.64

Note: HSECLK external crystal oscillator is 8MHz, and when fHCLK>8MHz, turn on PLL. Otherwise, turn off PLL.

5.7.3 Power consumption in sleep mode

Table 36 Power Consumption in Sleep Mode when the Program is Executed in Flash

Mode	Condition	f_{HCLK}	T_A=25℃，V_{DD}=3.3V				T_A=85℃，V_{DD}=3.6V			
			I_{DDA}(μA)		I_{DD}(mA）		I_{DDA}(μA)		I_{DD}(mA)	
			Typical value	Maximum value	Typical value	Maximum value	Typical value	Maximum value	Typical value	Maximum value
Sleep mode	HSECLK(1), enabling all peripherals	72MHz	226.9	231.4	4.02	4.09	245.3	250.6	4.09	4.16
		48MHz	178.2	182.2	2.91	2.98	193.1	197	2.96	3.01
		24MHz	135.6	139.4	1.85	1.87	149.1	153	1.92	1.94
		8MHz	123.7	127.2	1.16	1.17	137.1	140.8	1.22	1.24
	HSECLK(1), turn off all peripherals	72MHz	226.8	231.4	1.56	1.59	245.2	249.7	1.62	1.68
		48MHz	178.2	182.0	1.3	1.32	193	197.2	1.37	1.42
		24MHz	135.7	139.1	1.04	1.04	149.1	152.6	1.11	1.17
		8MHz	123.6	127.1	0.87	0.87	136.9	140.5	0.93	1
	HSICLK, enable all peripherals	64MHz	211.8	215.5	3.16	3.21	234.1	237	3.19	3.26
		48MHz	179.9	183.9	2.37	2.46	199	201.7	2.45	2.52
		24MHz	137.4	140.2	1.33	1.35	154	156.4	1.4	1.42
		8MHz	125.6	128.3	0.64	0.65	141.8	144.3	0.7	0.71
	HSICLK, turn off all peripherals	64MHz	211.9	215.5	0.94	0.96	234	237.2	1	1.02
		48MHz	179.9	183.3	0.77	0.78	198.8	201.7	0.83	0.85
		24MHz	137.4	140.5	0.51	0.53	153.8	156.4	0.57	0.59
		8MHz	125.3	128.3	0.34	0.35	141.6	144.3	0.4	0.41

Note: HSECLK external crystal oscillator is 8MHz, and when f_{HCLK}>8MHz, turn on PLL. Otherwise, turn off PLL.

Table 37 Power Consumption in Sleep Mode when the Program is Executed in SRAM

Mode	Condition	f_{HCLK}	T_A=25℃，V_{DD}=3.3V				T_A=85℃，V_{DD}=3.6V			
			I_{DDA}(μA)		I_{DD}(mA)		I_{DDA}(μA)		I_{DD}(mA)	
			Typical value	Maximum value	Typical value	Maximum value	Typical value	Maximum value	Typical value	Maximum value
Sleep mode	HSECLK(1), enabling all peripherals	72MHz	150.2	155.6	3.96	4.03	159.9	164.8	4.03	4.11
		48MHz	101.7	106.6	2.84	2.9	107.7	112.4	2.9	3
		24MHz	59	63.4	1.81	1.82	63.4	67.2	1.88	1.97
		8MHz	47	51.7	1.11	1.12	51.6	55.8	1.18	1.28
	HSECLK(1), turn off all peripherals	72MHz	150.3	155.3	1.52	1.55	159.7	164.2	1.6	1.67
		48MHz	101.7	106.3	1.27	1.29	107.6	112	1.33	1.42
		24MHz	59	63.6	1	1.01	63.5	67.4	1.08	1.16
		8MHz	46.9	51.5	0.83	0.84	51.6	55.5	0.9	1
	HSICLK, enable all peripherals	64MHz	211.4	214.1	3.13	3.21	234.1	237	3.27	3.35
		48MHz	179.3	181.9	2.36	2.41	198.8	201.4	2.53	2.58
		24MHz	136.9	138.8	1.33	1.35	154	156.2	1.45	1.5
		8MHz	124.9	126.9	0.64	0.65	141.8	144.2	0.73	0.76
	HSICLK, turn off all peripherals	64MHz	211.4	214.4	0.94	0.96	234.1	237.2	1.02	1.04
		48MHz	179.3	181.7	0.77	0.79	198.9	201.4	0.83	0.84
		24MHz	136.8	138.8	0.51	0.53	153.8	156.4	0.57	0.58
		8MHz	125	126.9	0.34	0.36	141.8	144.3	0.4	0.41

Note: HSECLK external crystal oscillator is 8MHz, and when f_{HCLK}>8MHz, turn on PLL. Otherwise, turn off PLL.

5.7.4 Power consumption in stop and standby mode

Table 38 Power Consumption in Stop and Standby Mode

Mode	Condition	T_A=25℃，V_{DD}=2.4V				T_A=25℃，V_{DD}=3.3V				T_A=85℃，V_{DD}=3.6V			
		I_{DDA} (μA)		I_{DD} (μA)		I_{DDA} (μA)		I_{DD} (μA)		I_{DDA} (μA)		I_{DD} (μA)	
		Typical value	Max value	Typical value	Max value	Typical value	Max value	Typical value	Max value	Typical value	Max value	Typical value	Max value
Stop mode	VDDA monitoring enabled, regulator in operating mode, low-speed and high-speed RC oscillators off	1.58	1.64	26.73	27.76	1.79	1.85	26.75	28.13	2.41	2.71	60.21	72.24
	VDDA monitoring disabled, regulator in low-power mode, low-speed and high-speed RC oscillators off	2.71	2.84	12.58	13.48	3.25	3.35	12.72	13.51	4.07	4.45	42.79	54.83
	VDDA monitoring enabled, regulator in low-power mode, low-speed and high-speed RC oscillators off	2.7	2.8	12.56	13.77	3.26	3.64	12.75	13.9	4.09	4.56	42.78	55.1
Stand by mode	VDDA monitoring enabled, low-speed RC oscillator and independent watchdog on	1.78	1.81	1.3	1.33	2.7	3.61	1.82	1.83	2.92	4.37	2.71	2.74
	VDDA monitoring enabled, low-speed RC oscillator and independent watchdog off	1.36	1.39	0.94	0.96	2.79	3.1	1.31	1.32	3.03	3.83	2.13	2.15
	VDDA monitoring disabled, low-speed RC oscillator and independent watchdog both on	1.78	1.81	1.28	1.3	3.29	3.61	1.8	1.82	3.59	4.39	2.7	2.75
	VDDA monitoring disabled, low-speed RC oscillator and independent watchdog both off	1.36	1.39	0.93	0.94	2.19	3.09	1.3	1.31	2.36	3.81	2.12	2.15

5.7.5 Peripheral power consumption

The HSECLK Bypass 1M is adopted as clock source, f_{PCLK}=f_{HCLK}=1M.

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table 39 Peripheral Power Consumption

Parameter	Peripheral	Typical value (1) T_A=25℃，V_{DD}=3.3V	Unit
AHB	DMA	0.106	mA/72MHz
	GPIOA	0.078	
	GPIOB	0.12	
	GPIOC	0.066	
	GPIOD	0.072	
	GPIOE	0.062	
	GPIOF	0.12	
	CRC	0.048	
APB1	TMR3	0.15	
	TMR6	0.062	
	TMR14	0.076	
	WWDT	0.082	
	IWDT	0.124	
	SPI2	0.08	
	USART2	0.1	
	I2C1	0.088	
	I2C2	0.078	
	PMU	0.08	
APB2	ADC	0.102	
	TMR1	0.174	
	SPI1	0.142	
	USART1	0.18	
	TMR15	0.126	
	TMR16	0.092	
	TMR17	0.09	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.8 Wake-up time in low-power mode

The measurement of wake-up time in low-power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 40 Wake-up Time in Low-power Mode(T_A=25℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{WUSLEEP}$	Wake-up from sleep mode	-	-	4 SYSCLK Cycles	-	μs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WUSTOP}	Wake up from the stop mode	-	22.4	22.75	22.9	
$t_{WUSTDBY}$	Wake up from standby mode	-	-	110	-	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.9 Port characteristics

5.9.1 I/O port characteristics

Table 41 DC Characteristics (V_{DD}=2.0~3.6V，T_A=-40~85℃)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IL}	Input low level voltage	TC and TTa I/O	-	-	$0.3V_{DD}$+0.1	V
		FT and FTf I/O	-	-	$0.476V_{DD}$+0.4	
		I/O pins except BOOT0 pin	-	-	$0.3V_{DD}$	
V_{IH}	Input high level voltage	TC and TTa I/O	$0.447V_{DD}$+0.402	-	-	V
		FT and FTf I/O	$0.5V_{DD}$+0.2	-	-	
		I/O pins except BOOT0 pin	0.7 V_{DD}	-	-	
V_{hys}	Schmidt trigger hysteresis	TC and TTa I/O	200	-	280	mV
		FT and FTf I/O	300	-	300	
I_{lkg}	Input leakage current	V_{SS}≤V_{IN}≤V_{DDIOx} Standard I / O port	-	-	±0.1	μA
		V_{IN}=5V, FT I/O	-	-	70	
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistance	V_{IN}=V_{DDIOx}	30	40	50	kΩ

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) Some pins have no Schmidt trigger function.

Table 42 AC Characteristics

OSSELy[1:0] Configuration of	Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
x0 (2MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD}=2.4~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output high to low fall time	C_L=50 pF, V_{DD}=2.4~3.6V	-	125	ns
	$t_{r\ (IO)out}$	Output rise time from low to high level		-	125	
01 (10MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD}=2.4~3.6V	-	10	MHz
	$t_{f(IO)out}$	Output high to low fall time	C_L=50 pF, V_{DD}=2.4~3.6V	-	25	ns
	$t_{r\ (IO)out}$	Output rise time from low to high level		-	25	
11 (50MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=30 pF, V_{DD}=2.7~3.6V	-	50	MHz
	$t_{f(IO)out}$	Output high to low fall time	C_L=30 pF, V_{DD}=2.7~3.6V	-	5	ns
	$t_{r\ (IO)out}$	Output rise time from low to high level		-	5.5	

Note:

(1) The speed of the I/O port can be configured via OSSELy.

(2) The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 15 I/O AC Characteristics Definition

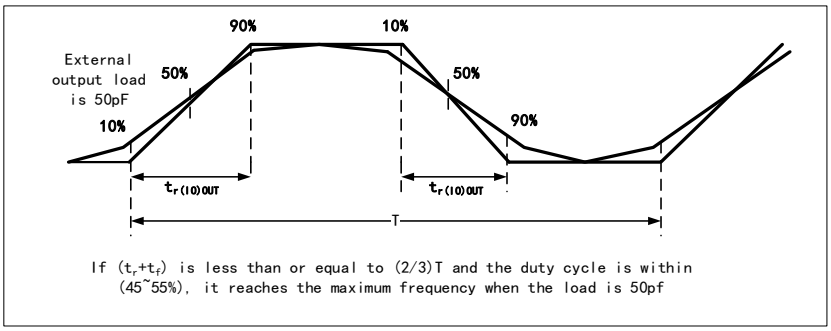


Table 43 Output Drive Voltage Characteristics (V_{DD}=2.7~3.6V，T_A=-40~85℃)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=8 mA V_{DDIOx}≥2.7V	-	0.4	V
V_{OH}	I/O pin outputs high voltage		V_{DDIOx}-0.4	-	
V_{OL}	I/O pin outputs low voltage	$\|I_{IO}\|$=20 mA V_{DDIOx}≥2.7V	-	1.3	
V_{OH}	I/O pin outputs high voltage		V_{DDIOx}-1.3	-	

5.9.2 NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}.

Table 44 NRST Pin Characteristics (V_{DD}=2.7~3.6V，T_A=-40~85℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low voltage	-	-	-	$0.31V_{DD}$+0.065	V
$V_{IH(NRST)}$	NRST input high voltage	-	$0.446V_{DD}$+0.405			
$V_{hys(NRST)}$	Voltage hysteresis of NRST Schmitt trigger	-	-	300	-	mV
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.10 Communication peripherals

5.10.1 I2C peripheral characteristics

To achieve maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz. To achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

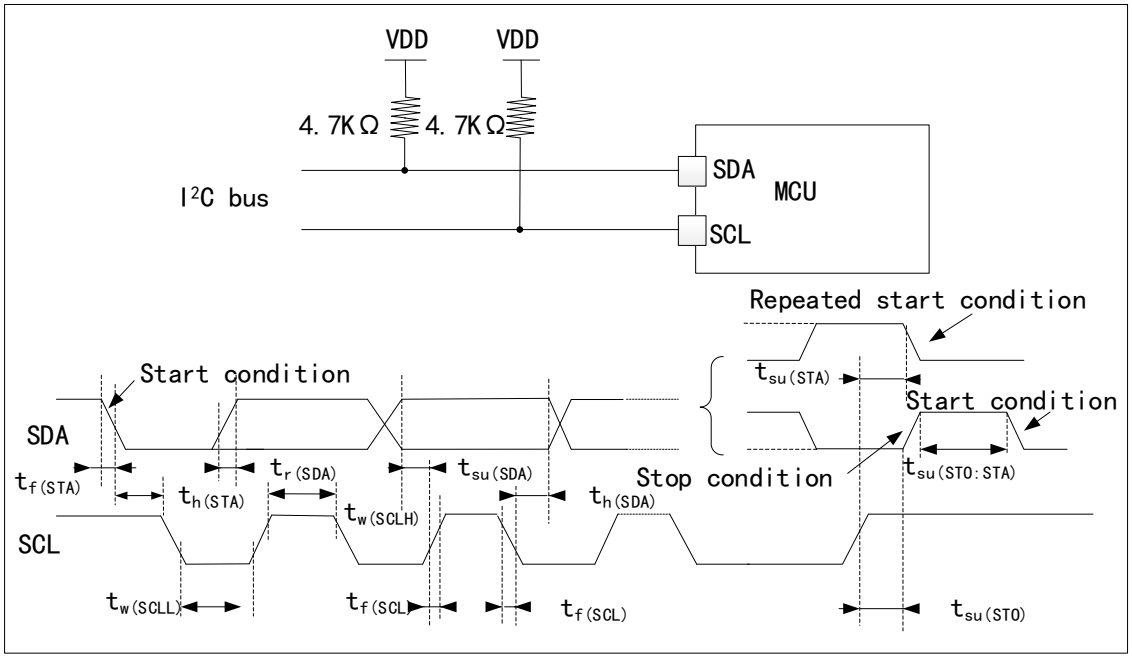
- Standard mode (Sm): bit rate up to 100kbit/s
- Fast mode (Fm): bit rate up to 400 kbit/s
- Ultra fast mode (Fm+): bit rate up to 1Mbit/s

Table 45 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Ultrafast I2C		Unit
		Min	Max	Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.84	-	1.21	-	0.52	-	μs
$t_{w(SCLH)}$	SCL clock high time	5.01	5.04	0.71	0.76	0.36	0.4	
$t_{su(SDA)}$	SDA setup time	4460	-	860	-	311.11	318.89	ns
$t_{h(SDA)}$	SDA data hold time	103	181	0	252	0	145	
$t_{r(SDA)}$/	SDA rise time	-	500	427.85	485.82	373.06	402.26	
$t_{r(SC\ L)}$	SCL rise time			420.24	470.94	367.04	461.86	
$t_{f(SDA)}$	SDA fall time	-	9.86	-	8.12	-	4	
$t_{f(SCL)}$	SCL fall time						4.88	
$t_{h(STA)}$	Start condition hold time	4.92	-	1	-	0.33	-	μs
$t_{su(STA)}$	Setup time of repeated start condition	4.78	4.91	1.21	-	0.6	-	
$t_{su(STO)}$	Setup time of stop condition	4.50	-	0.9	0.97	0.54	-	
$t_{w(STO:STA)}$	Time from stop condition to start condition (the bus is idle)	4.67	-	1.37	-	0.77	-	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 16 Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.10.2 SPI peripheral characteristics

Table 46 SPI Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Condition	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	holotype	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 15pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	223	-	ns
$t_{h(NSS)}$	NSS holding time	Slave mode	56.67	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Main mode, f_{PCMU} = 36MHz, Prescaler coefficient =4	54	57	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	holotype	12	-	ns
		Slave mode	20	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input holding time	holotype	33.67	-	ns
		Slave mode	33	-	
$t_{a(SO)}$	Data output access time	In slave mode, f_{PCLK} = 20MHz	-	17	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode	-	18	ns

Symbol	Parameter	Condition	Min	Max	Unit
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	-	16	ns
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)	-	6	ns
$t_{h(SO)}$	Data output holding time	Slave mode (after enable edge)	11.5	-	ns
$t_{h(MO)}$		Master mode (after enable edge)	2	-	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 17 SPI Timing Diagram - Slave Mode and CPHA=0

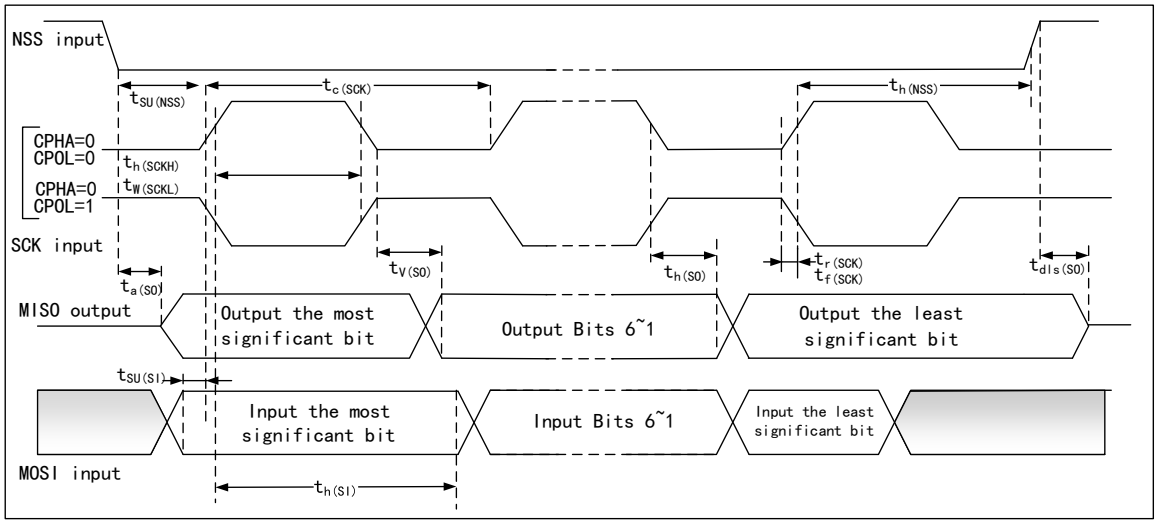
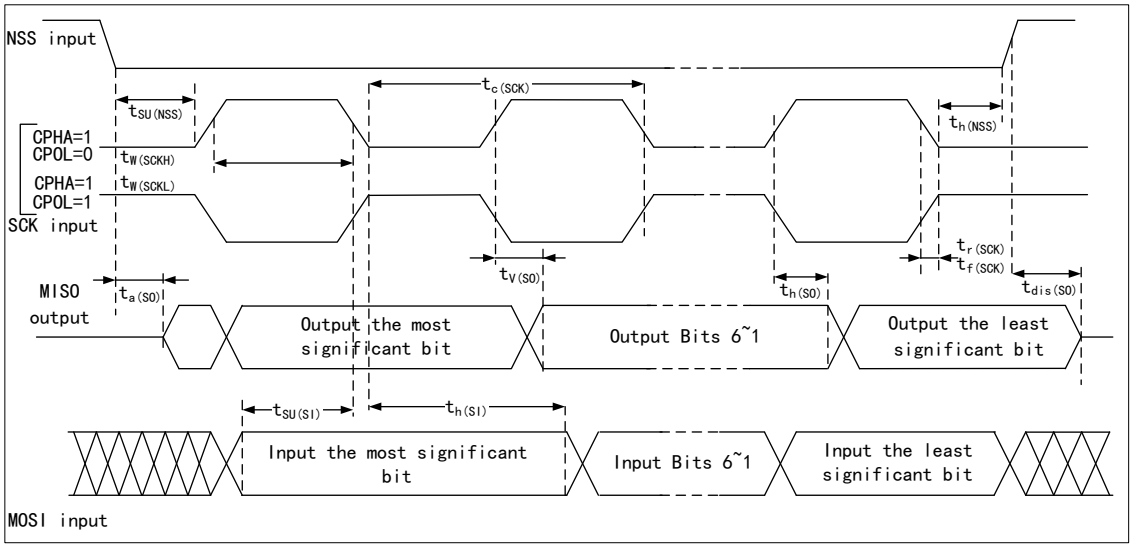
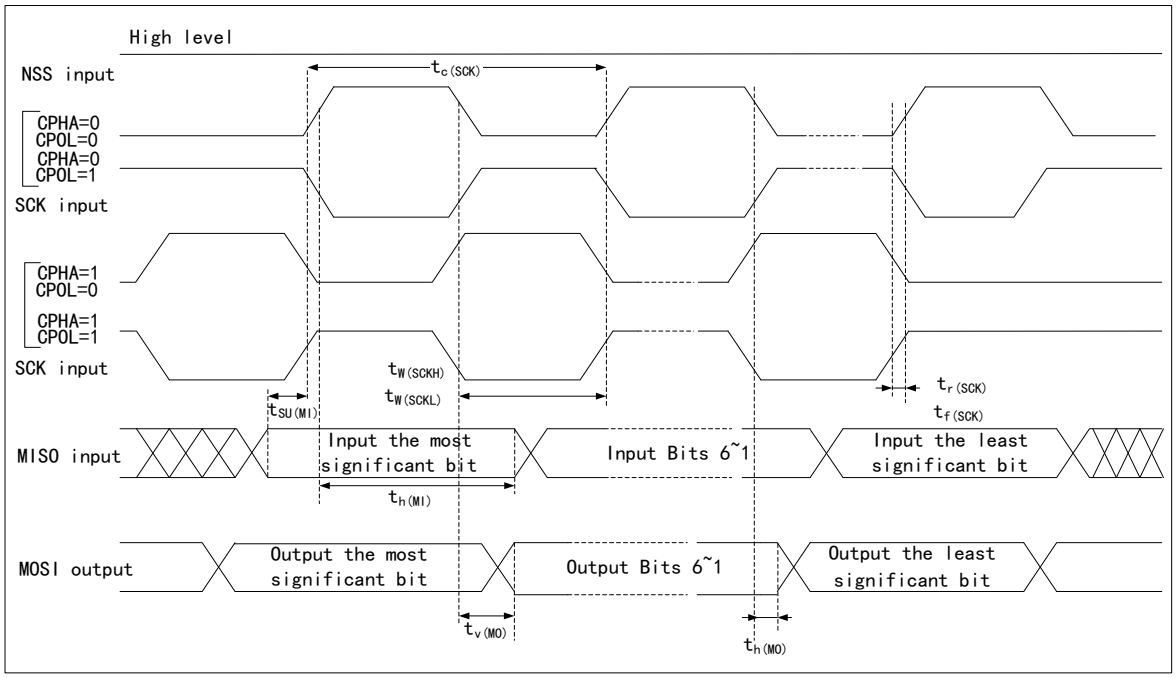


Figure 18 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 19 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.11 Analog peripherals

5.11.1 ADC

Test parameter description:

- Sampling rate: the number of conversion of analog quantity to digital quantity by ADC per second, Sample rate=ADC clock/(number of sampling periods + number of conversion periods)

5.11.1.1 12-bit ADC characteristics

Table 47 12-bit ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply voltage	-	2.4	-	3.6	V
I_{DDA}	ADC power consumption	V_{DDA}=3.3V，f_{ADC}=14MHz，Sample time=1.5 f_{ADC}	-	1	-	mA
f_{ADC}	ADC frequency	-	0.6	-	14	MHz
C_{ADC}	Internal sampling and holding capacitance	-	-	8	-	pF
R_{ADC}	Sampling resistor	-	-	-	1000	Ω
t_S	Sampling time	f_{ADC}=14MHz	0.107	-	17.1	μs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		-	1	-	18	$1/f_{ADC}$
T_{CONV}	Sampling and conversion time	f_{ADC}=14MHz 12-bit resolution	2.4	-	3.6	μs

Table 48 12-bit ADC Accuracy

Symbol	Parameter	Conditions	Typ	Max	Unit
E_T	Composite error	f_{PCLK}=72MHz, f_{ADC}=14MHz, V_{DDA}=2.4V-3.6V T_A=-40℃~85℃	±3.10	±3.97	LSB
E_O	Offset error		±0.29	±0.95	
E_G	Gain error		±1.59	±2.69	
E_D	Differential linear error		±1.03	±1.46	
E_L	Integral linear error		±1.78	±2.56	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.11.2 Temperature Sensor Characteristics

Table 49 Temperature Sensor Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
T_{SENSOR}	Temperature sensor error	-	±1	±2	℃
Avg_Slope	Average slope	4.0	4.3	4.6	mV/℃
V_{30}	Reference voltage at 30℃(±5℃)	1.34	1.43	1.52	V
t_{START} + t_{s_temp}	start Sampling time	4-	-	27.1	μs

5.11.2.1 Test of Built-in Reference Voltage Characteristics

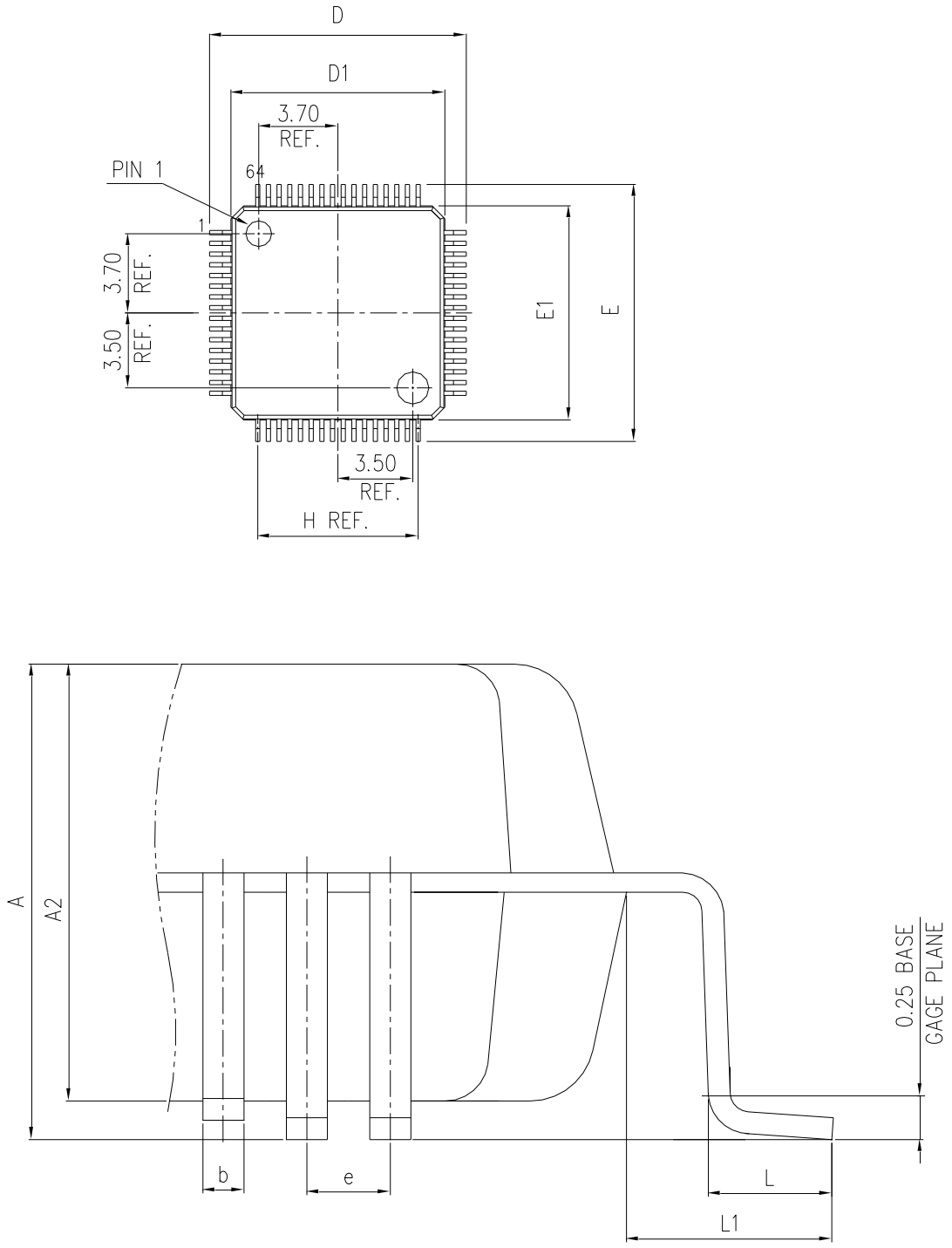
Table 50 Built-in Reference Voltage Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Built-in Reference Voltage	-40℃ < T_A < +85℃	1.18	1.20	1.22	V
t_{START}	Reference voltage buffer start time	-	-	-	15	μs
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	4	-	-	μs
ΔV_{RERINT}	Built-in reference voltage extends to temperature range	V_{DDA}=3.3V	-	-	10	mV

6 Package Information

6.1 LQFP64 package information

Figure 20 LQFP64 Package Diagram



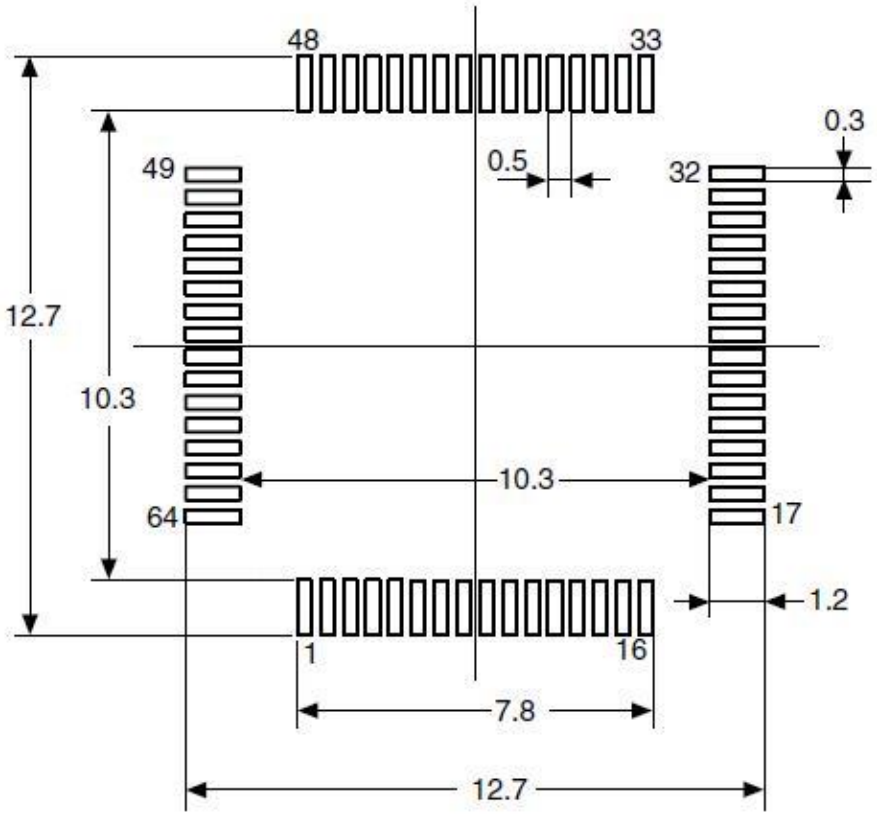
(1) The figure is not drawn to scale.
(2) All pins should be soldered to the PCB.

Table 51 LQFP64 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	26.000±0.200	LEAD TIP TO TIP
4	D1	24.000±0.100	PKG LENGTH
5	E	26.000±0.200	LEAD TIP TO TIP
6	E1	24.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H（REF）	（21.50）	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

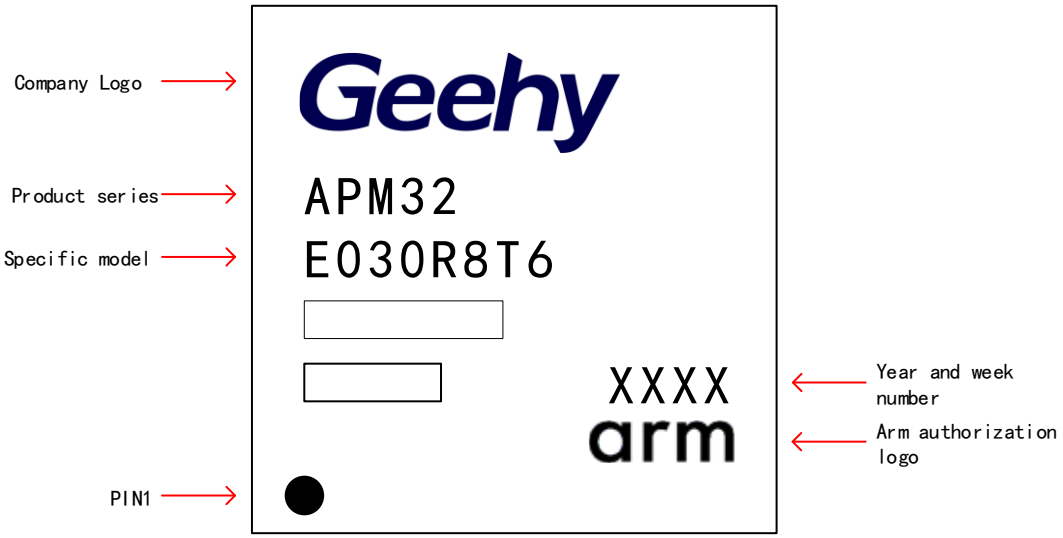
Note: Dimensions are marked in millimeters.

Figure 21 LQFP64 -64 Pins, 10 x10mm Welding Layout Recommendations



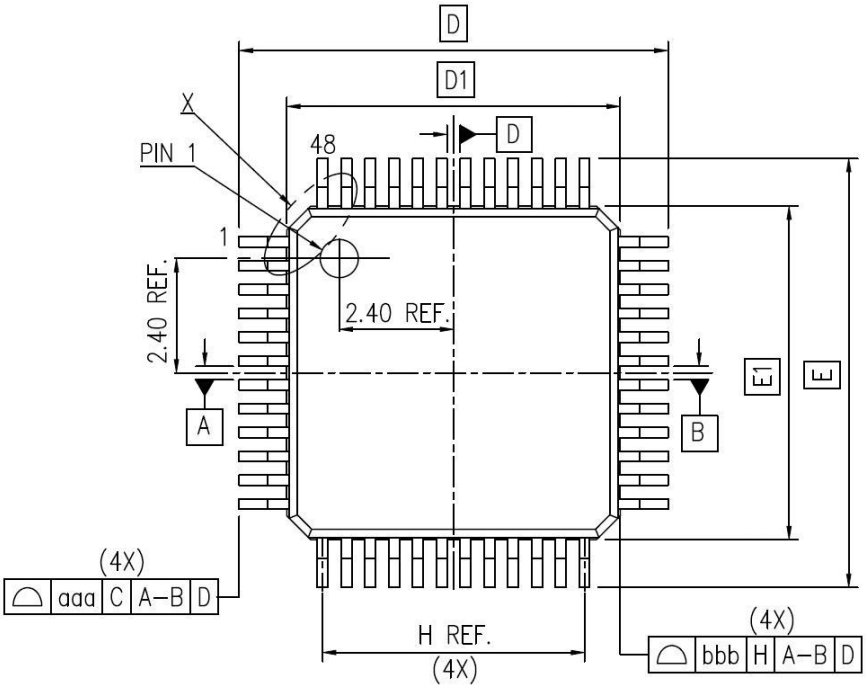
Note: Dimensions are in millimeters.

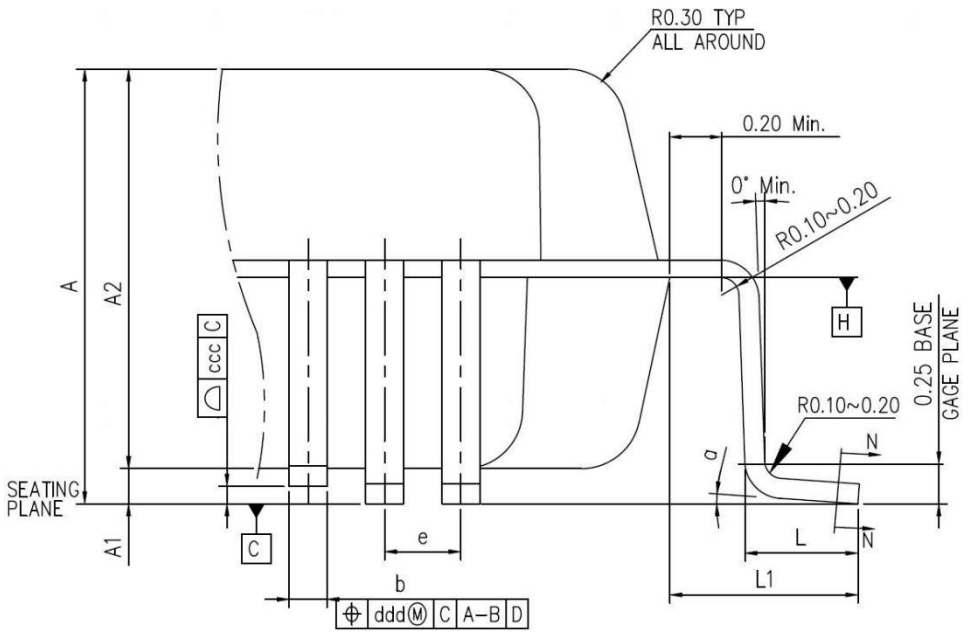
Figure 22 LQFP64 -64 Pins, 10 x10mm Schematic Diagram



6.2 LQFP48 package information

Figure 23 LQFP48 Package Diagram





(1) The figure is not drawn to scale.

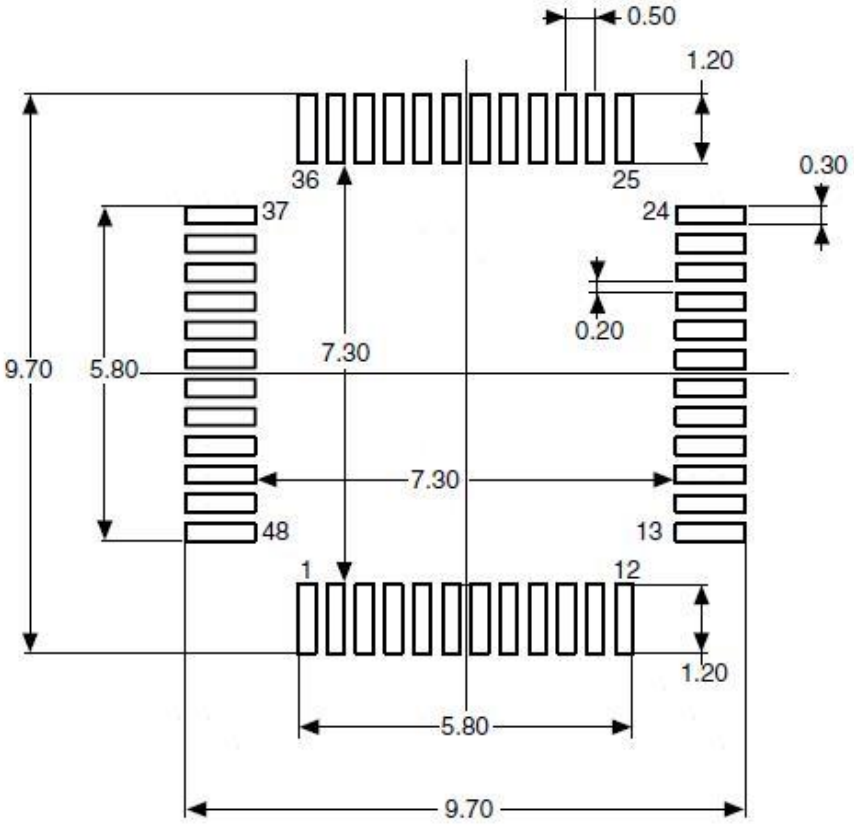
(2) All pins should be soldered to the PCB.

Table 52 LQFP48 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)			
S/N	SYM	DIMENDIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.1±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	9.00±0.20	LEAD TIP TO TIP
5	D1	7.00±0.10	PKG LENGTH
6	E	9.00±0.20	LEAD TIP TO TIP
7	E1	7.00±0.10	PKG WDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF	LEAD LENGTH
10	T	0.15	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.02	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	H(REF.)	(5.50)	CUM. LEAD PITCH
17	aaa	0.2	PROFILE OF LEAD TIPS
18	bbb	0.2	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

Note: Dimensions are marked in millimeters.

Figure 24 LQFP48-48 Pins, 7 x 7mm Welding Layout Recommendations

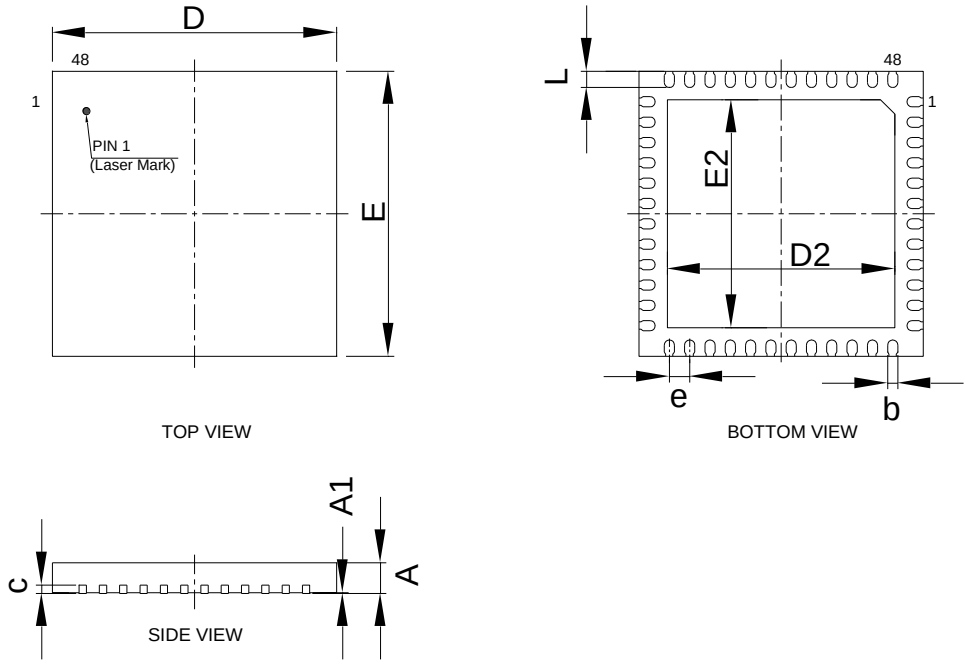


Note: Dimensions are marked in millimeters.

Figure 25 LQFP48 -48 Pins, 7 x7mm Schematic Diagram

6.3 QFN48 package information

Figure 26 QFN48 Package Diagram



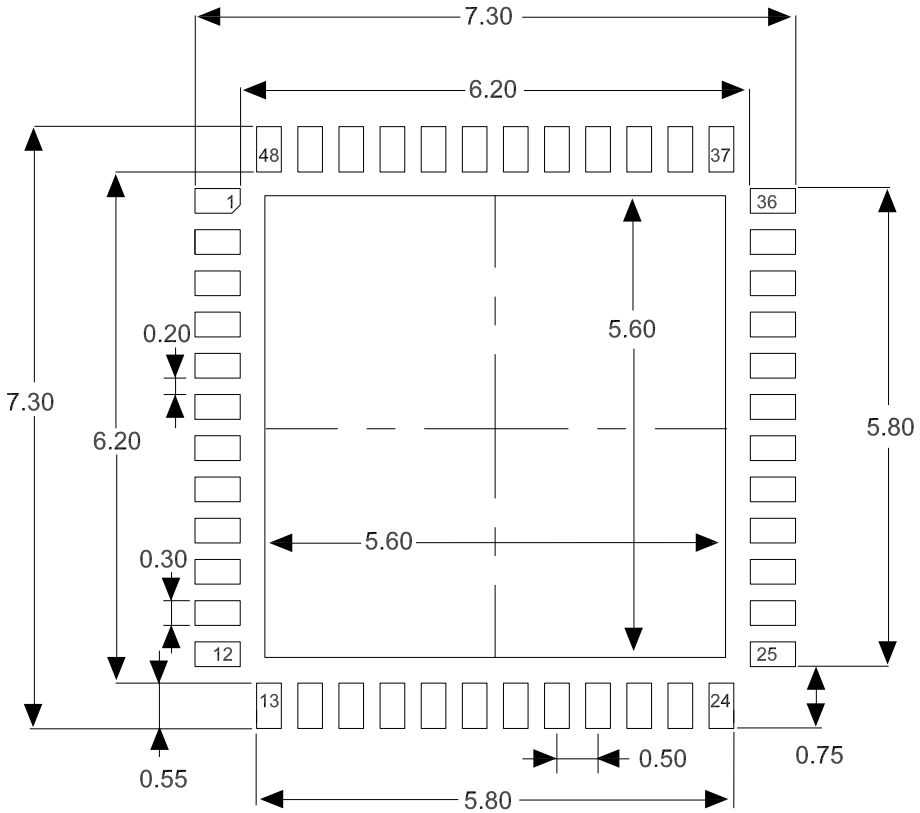
Note: The Figure is not drawn to scale.

Table 53 QFN48 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
e	0.50BSC		
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
L	0.35	0.40	0.45

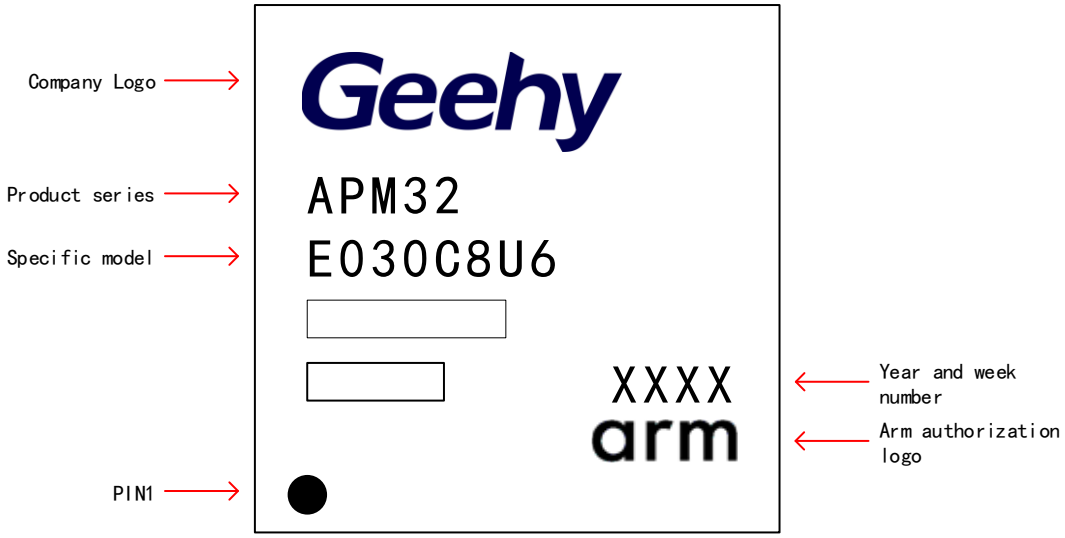
Note: Dimensions are marked in millimeters.

Figure 27 QFN48, Welding Layout Recommendations



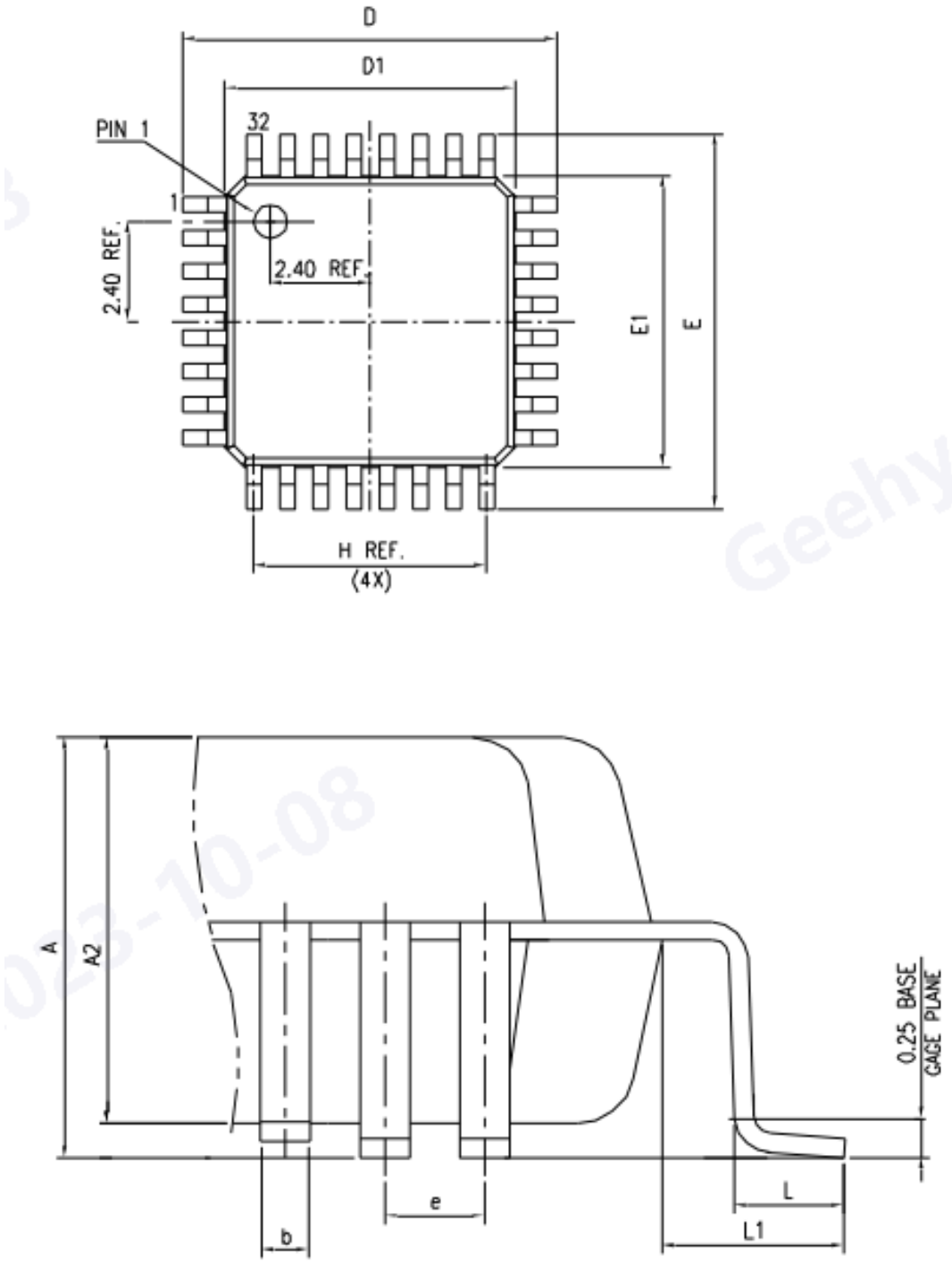
Note: Dimensions are marked in millimeters.

Figure 28 QEN48 - 48 Pins, 7 x 7mm Package Schematic Diagram



6.4 LQFP32 package information

Figure 29 LQFP32 Package Diagram



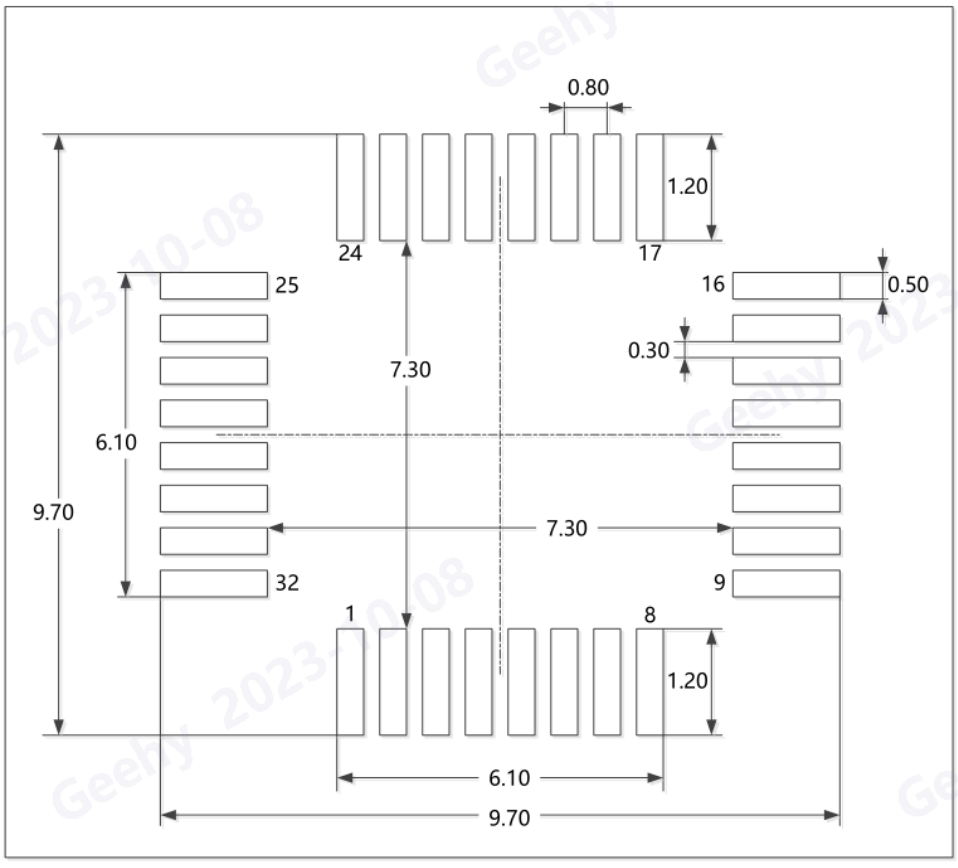
Note: The Figure is not drawn to scale.

Table 54 LQFP32 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.6	OVERALL HEIGHT
2	A2	1.40±0.05	PKG THICKNESS
3	D	9.00±0.20	LEAD TIP TO TIP
4	D1	7.00±0.10	PKG LENGTH
5	E	9.00±0.20	LEAD TIP TO TIP
6	E1	7.00±0.10	PKG WIDTH
7	L	0.60±0.15	FOOT LENGTH
8	L1	1.00 REF.	LEAD LENGTH
9	E	0.80 BASE	LEAD PITCH
10	H(REF.)	(5.60)	GUM.LEAD PITCH
11	b	0.370±0.080/0.070	LEAD WIDTH

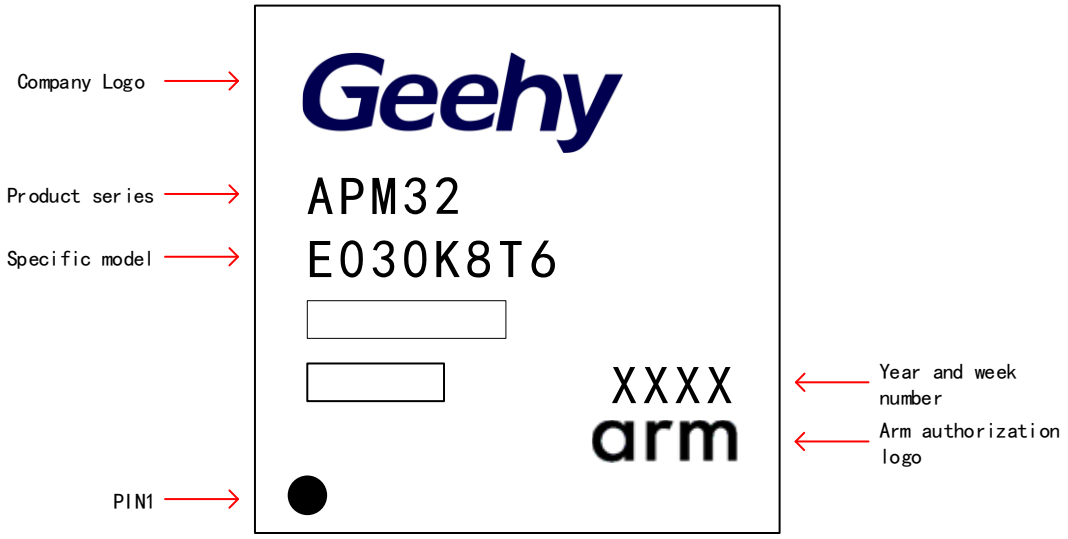
Note: The value in inches is converted from mm to 4 decimal places.

Figure 30 LQFP32 Welding Layout Recommendations



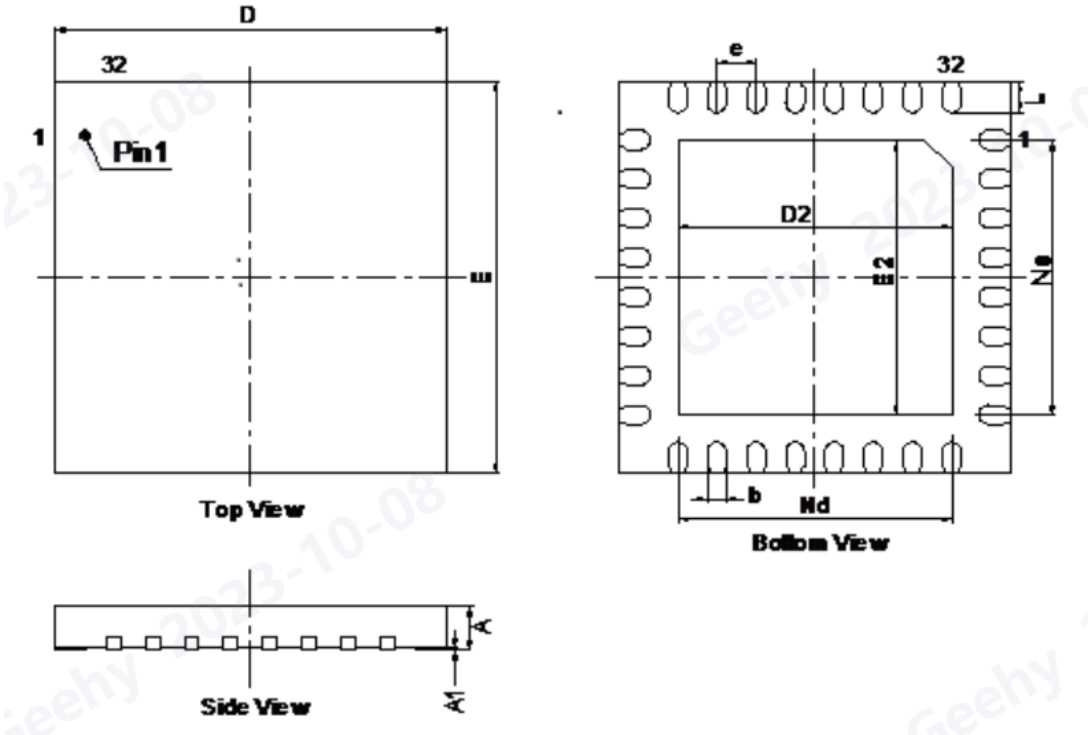
Note: Dimensions are marked in millimeters.

Figure 31 LQFP32 - 32 Pins, 9 x 9mm Package Schematic Diagram



6.5 QFN32 package information

Figure 32 QFN32 Package Diagram



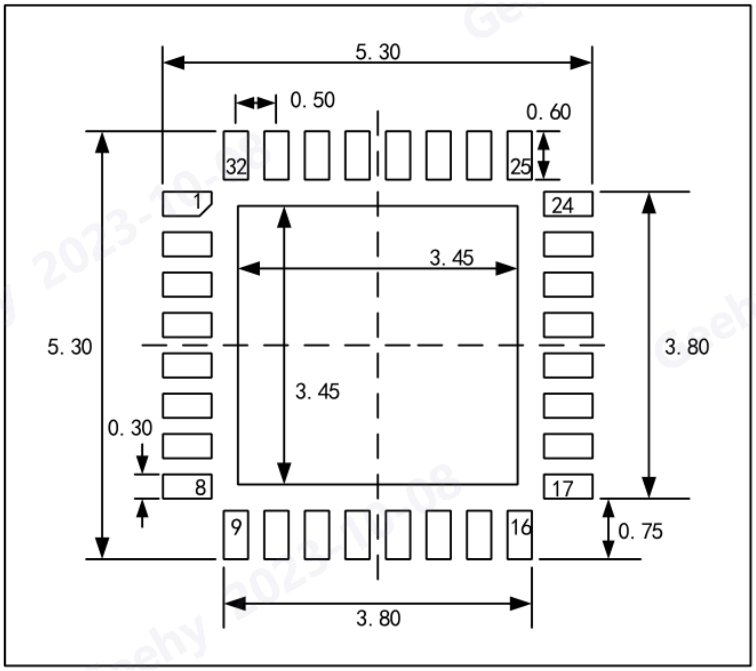
Note: The Figure is not drawn to scale.

Table 55 QFN32 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.5	0.55	0.6
A1	0	0.02	0.05
b	0.19	0.24	0.29
D	4.9	5	5.1
D2	3.4	3.5	3.6
e	0.50BSC		
Nd	3.50BSC		
E	4.9	5	5.1
E2	3.4	3.5	3.6
Ne	3.50BSC		
L	0.35	0.4	0.45

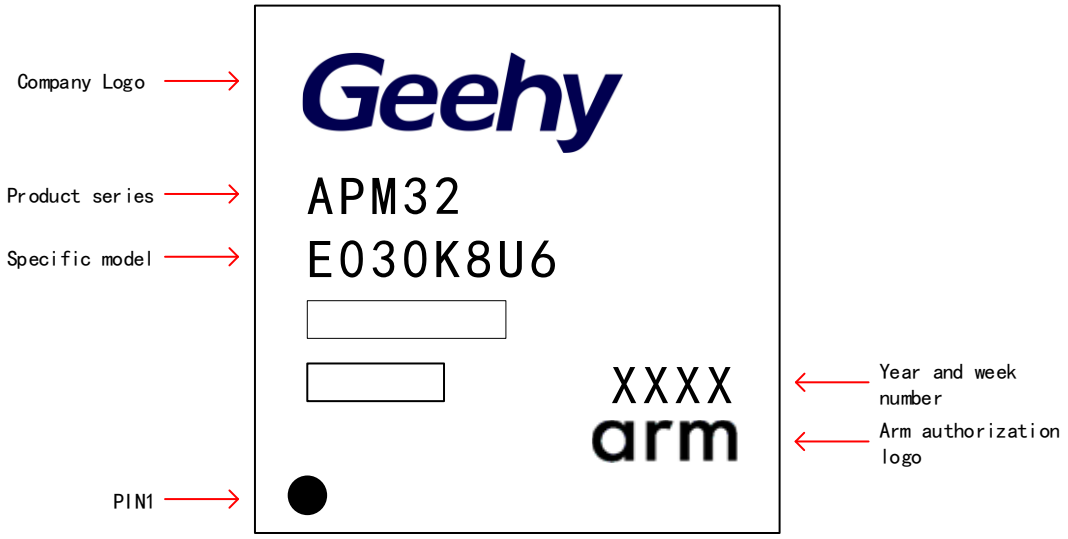
Note: The value in inches is converted from mm to 4 decimal places.

Figure 33 QFN32 Welding Layout Recommendations



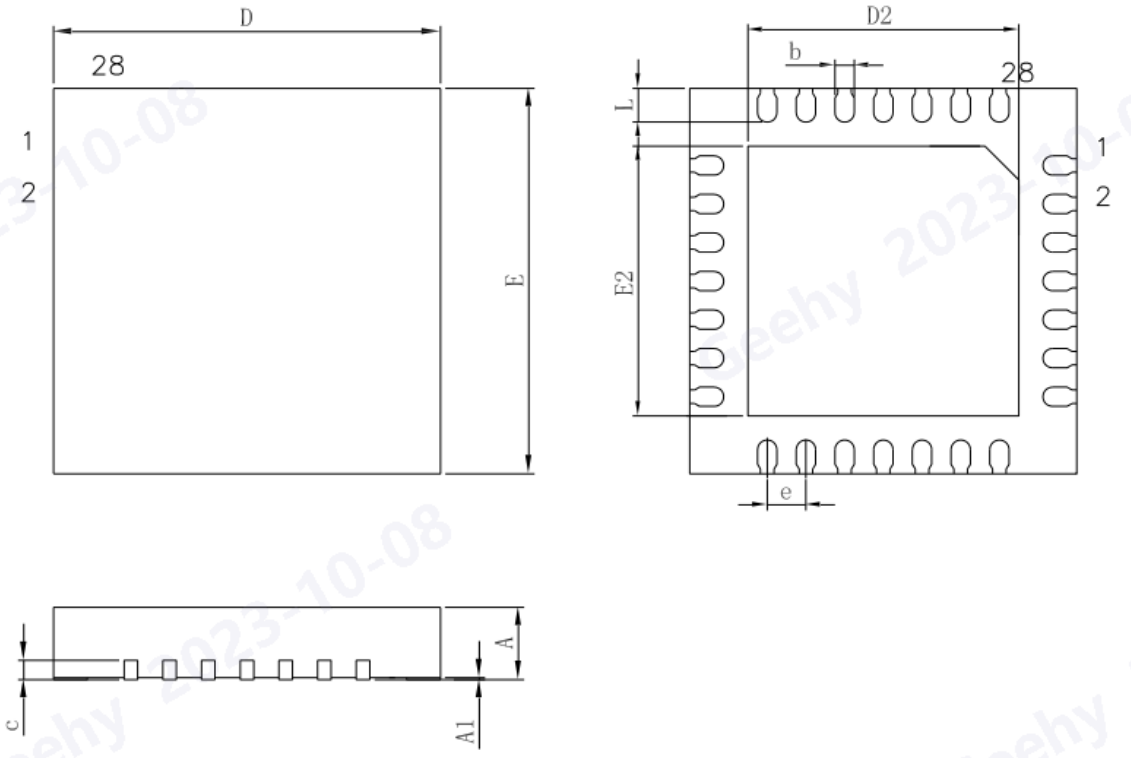
Note: Dimensions are marked in millimeters.

Figure 34 QFN32 - 32 Pins, 5 x 5mm Package Schematic Diagram



6.6 QFN28 package information

Figure 35 LQFP32 Package Diagram



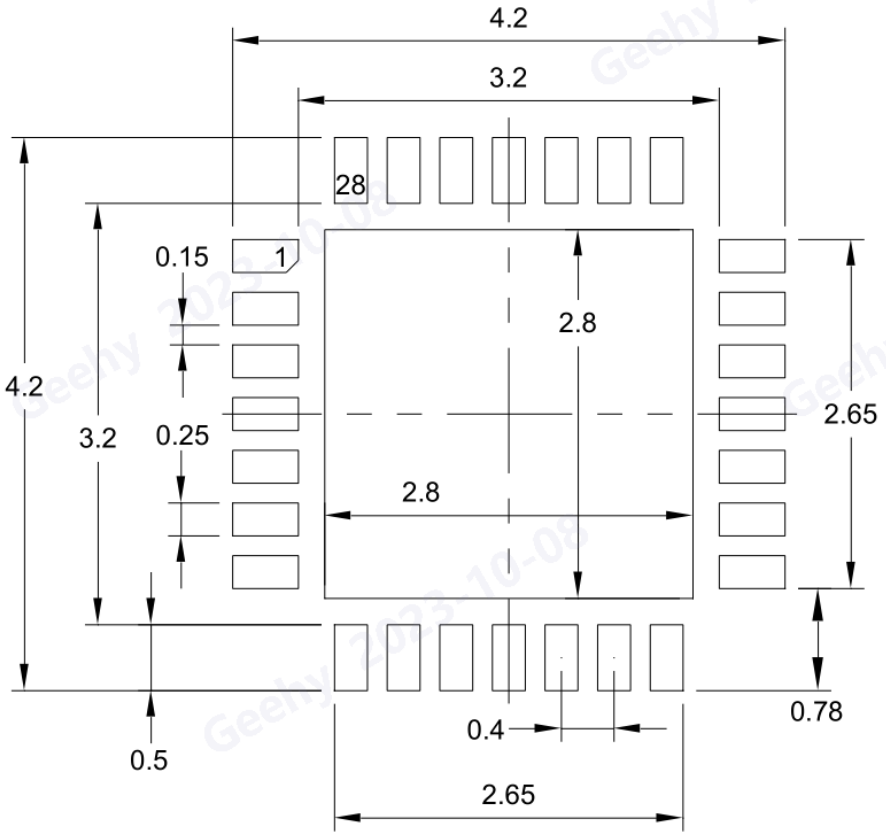
Note: The Figure is not drawn to scale.

Table 56 QFN28 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40 BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.30	0.35	0.40

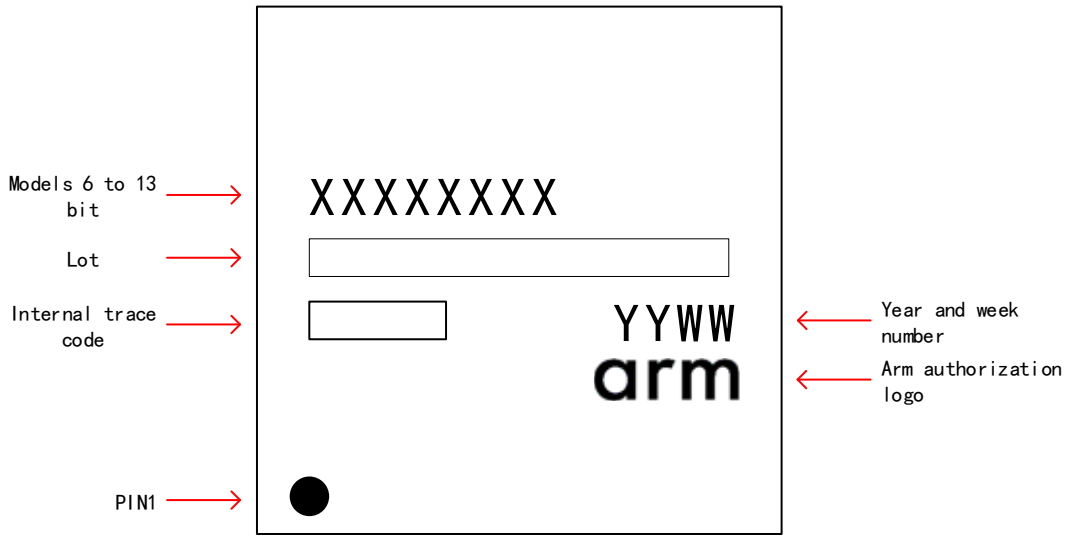
Note: The value in inches is converted from mm to 4 decimal places.

Figure 36 QFN28 Welding Layout Recommendations



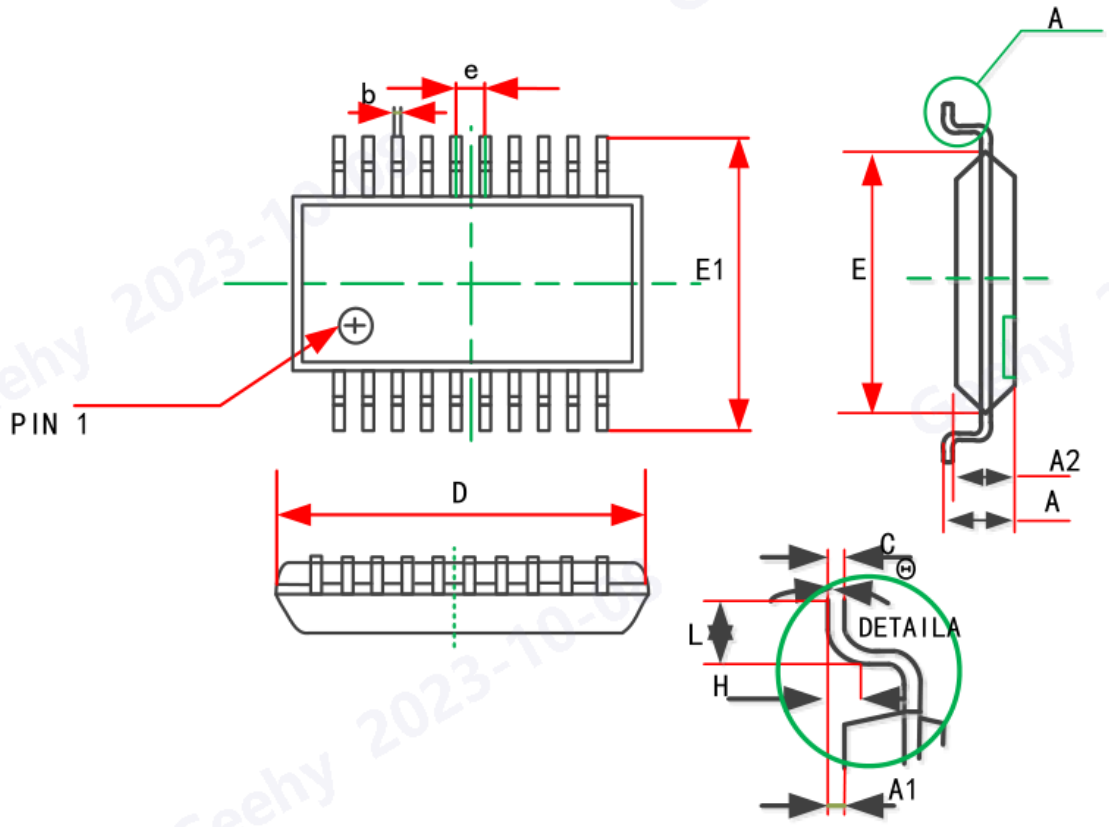
Note: Dimensions are marked in millimeters.

Figure 37 QFN28 - 28Pins, 4 x 4mm Package Schematic Diagram



6.7 TSSOP20 package information

Figure 38 LQFP32 Package Diagram



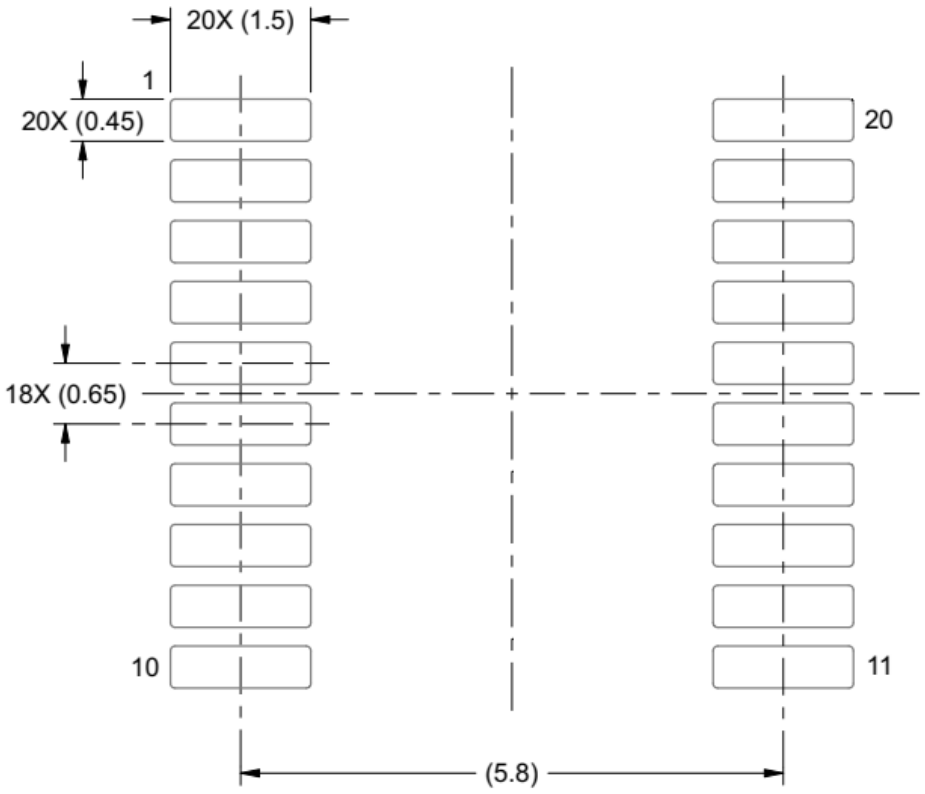
Note: The Figure is not drawn to scale.

Table 57 TSSOP20 Package Data

SYMBOL	Dimensions in Millimeters		Dimensions in Inches	
	MIN	MAX	MIN	MAX
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A	-	1.200	-	0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1	7	1	7

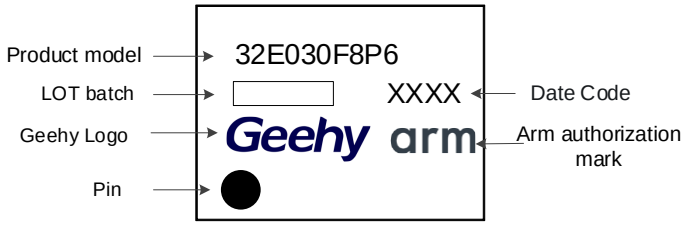
Note: The value in inches is converted from mm to 4 decimal places.

Figure 39 TSSOP20 Recommended Welding Layout



Note: Dimensions are marked in millimeters.

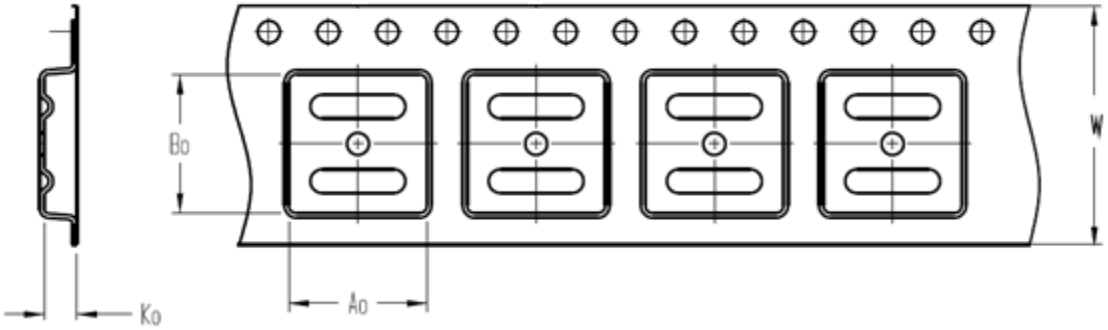
Figure 40 TSSOP20 – 20 Pins,4.4 x 6.5mm Package Schematic Diagram



7 Packaging Information

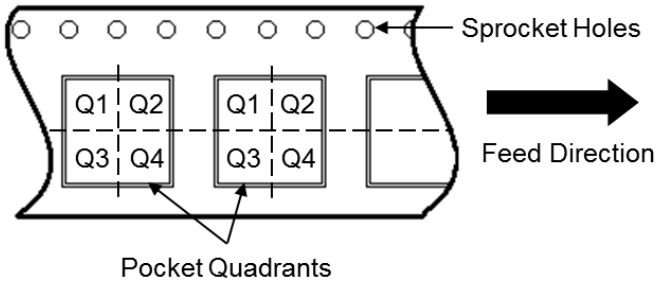
7.1 Reel packaging

Figure 41 Specification Drawing of Reel Packaging

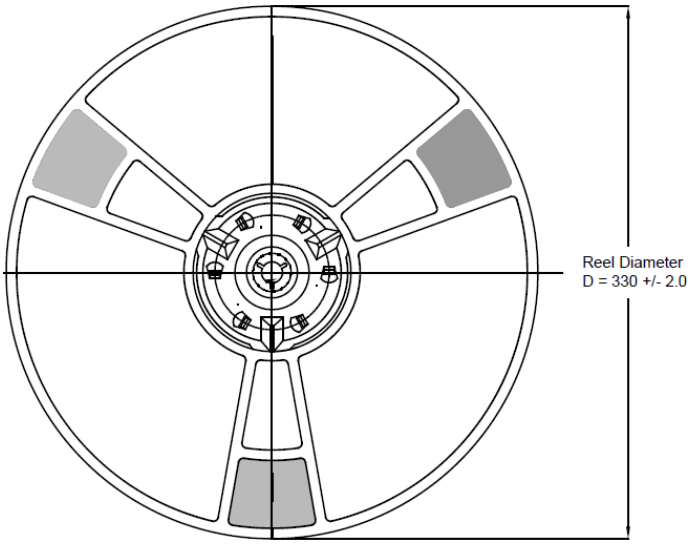


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



All photos are for reference only, and the appearance is subject to the product.

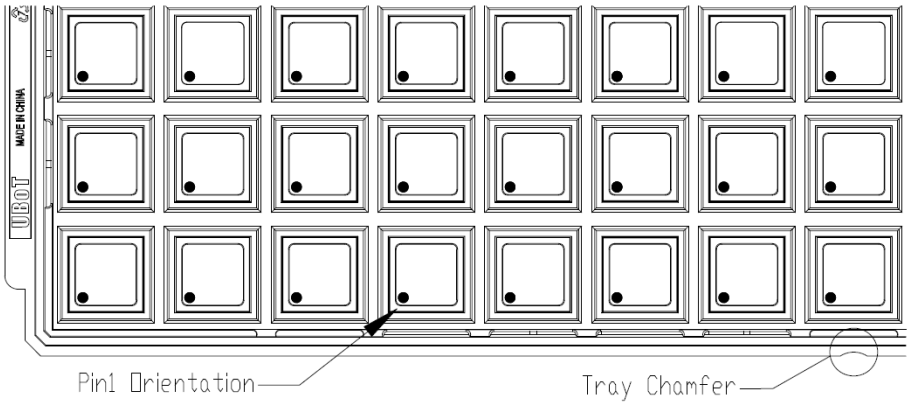
Table 58 Reel Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	Reel Diameter（mm）	A0（mm）	B0（mm）	K0（mm）	W（mm）	Pin1 Quadrant
APM32E030R8T6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32E030C8T6	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32E030C8T7	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32E030K8T6	LQFP	32	2000	330	9.3	9.3	2.2	16	Q1
APM32E030K8U6	QFN	32	5000	330	5.3	5.3	0.8	12	Q1
APM32E030F8P6	TSSOP	20	4000	330	6.7	6.7	1.3	16	Q1

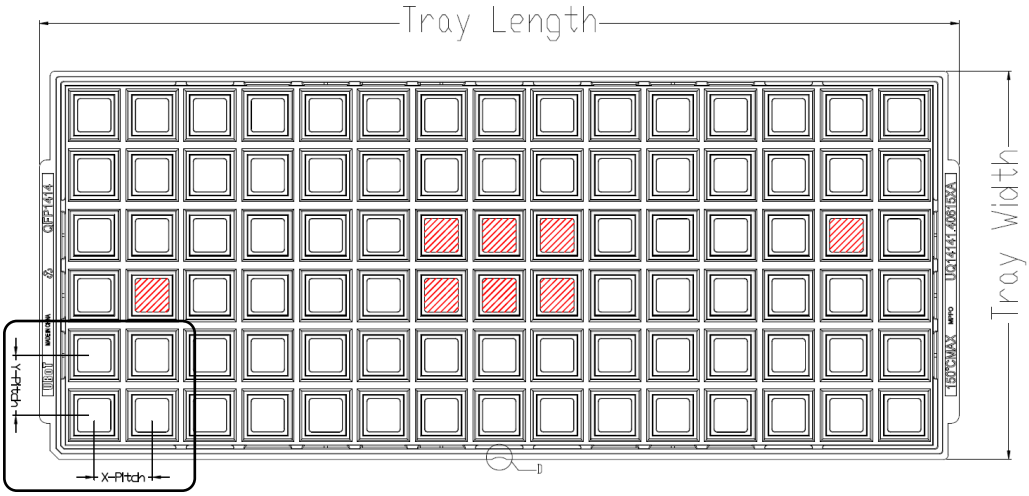
Note: SPQ= Minimum package quantity

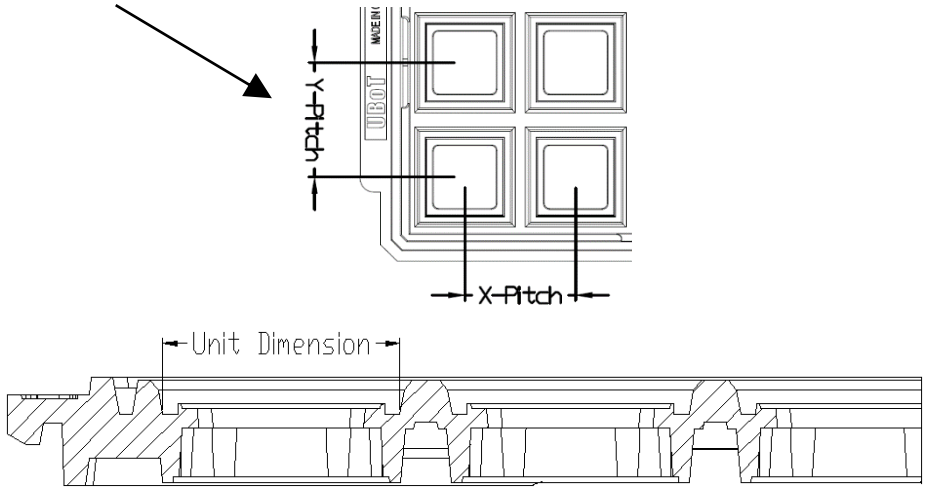
7.2 Tray packaging

Figure 42 Tray Packaging Diagram



Tray Dimensions





All photos are for reference only, and the appearance is subject to the product

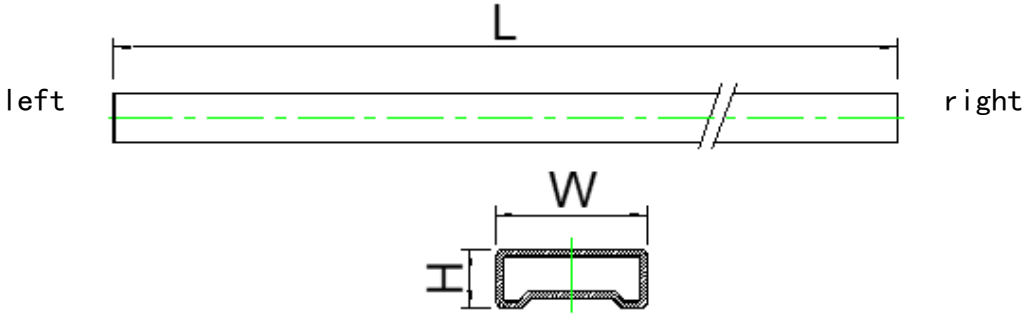
Table 59 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension （mm）	Y-Dimension （mm）	X-Pitch （mm）	Y-Pitch （mm）	Tray Length （mm）	Tray Width （mm）
APM32E030R8T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32E030C8T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32E030C8T6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32E030K8T6	LQFP	32	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32E030C8U6	QFN	48	4900	6.25	6.25	8.8	9.2	322.6	135.9
APM32E030K8U6	QFN	32	4900	5.2	5.2	8.7	9.0	322.6	135.9
APM32E030G8U6	QFN	28	4900	4.2	4.2	8.8	9.2	322.6	135.9

Note: SPQ= Minimum package quantity

7.2.1 Tube packing

Figure 43 Tube packing diagram



All photos are for reference only, the appearance is subject to the product.

Table 60 Tube Packaging Parameter Specification Table

Device	Package Type	Pins	Qty Per Tube	SPQ	L （mm）	W （mm）	H （mm）
APM32E030F8P6	TSSOP	20	46	14720	327	8.5	3.2

Note: SPQ= Minimum package quantity

8 Ordering Information

Figure 44 APM32E030x8 Series Ordering Information Diagram

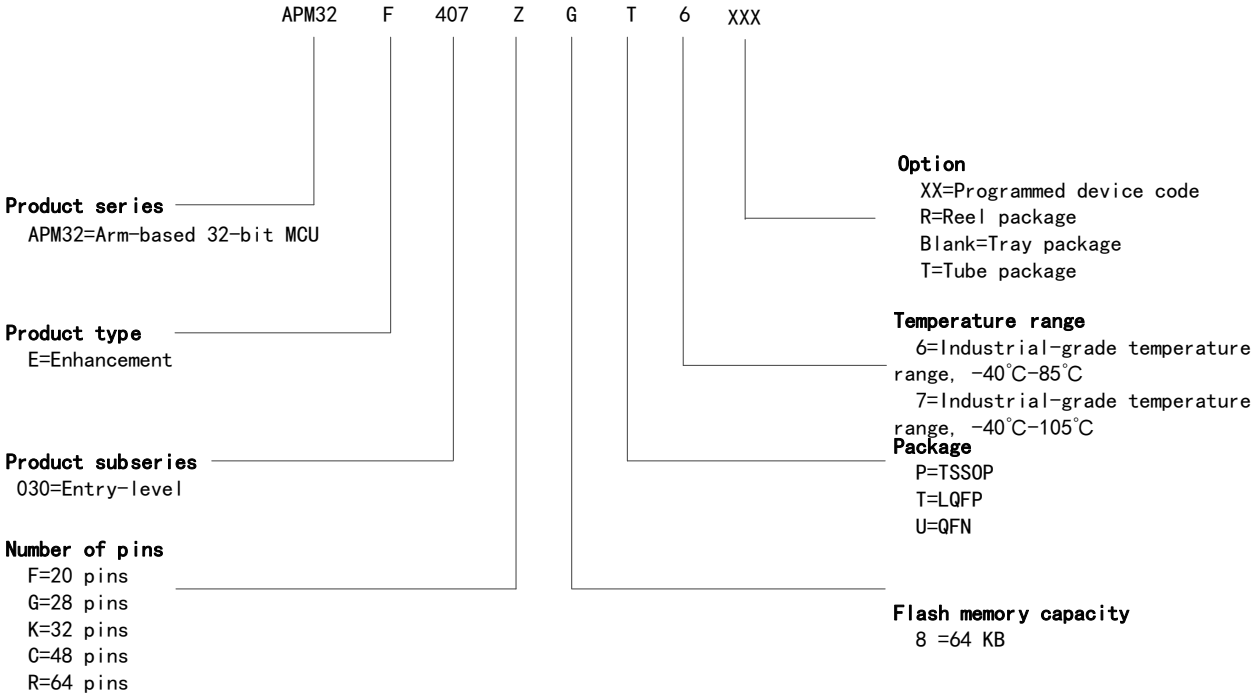


Table 61 Ordering Information Table

Order code	FLASH（KB）	SRAM（KB）	Package	SPQ	Range of temperature
APM32E030R8T6-R	64	8	LQFP64	1000	Industrial grade -40℃~85℃
APM32E030C8T6-R	64	8	LQFP48	2000	Industrial grade -40℃~85℃
APM32E030C8T7-R	64	8	LQFP48	2000	Industrial grade -40℃~105℃
APM32E030K8T6-R	64	8	LQFP32	2000	Industrial grade -40℃~85℃
APM32E030K8U6-R	64	8	QFN32	5000	Industrial grade -40℃~85℃
APM32E030F8P6-R	64	8	TSSOP20	4000	Industrial grade -40℃~85℃
APM32E030R8T6	64	8	LQFP64	1600	Industrial grade -40℃~85℃
APM32E030C8T6	64	8	LQFP48	2500	Industrial grade -40℃~85℃
APM32E030C8T7	64	8	LQFP48	2500	Industrial grade -40℃~105℃
APM32E030K8T6	64	8	LQFP32	2500	Industrial grade -40℃~85℃
APM32E030C8U6	64	8	QFN48	4900	Industrial grade -40℃~85℃
APM32E030K8U6	64	8	QFN32	4900	Industrial grade -40℃~85℃
APM32E030G8U6	64	8	QFN28	4900	Industrial grade -40℃~85℃
APM32E030F8P6-T	64	8	TSSOP20	14720	Industrial grade -40℃~85℃

Note: SPQ= Minimum package quantity

9 Commonly Used Function Module Denomination

Table 62 Commonly Used Function Module Denomination

Full name	Abbreviations
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External interrupt	EINT
General-purpose IO	GPIO
Multiplexing IO	AFIO
Wake-up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller local area network	CAN
I2C Interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC

10 Version History

Table 63 Document Version History

Date	Version	Change History
November 2024	1.0	New
February 2025	1.1	Update data of electrical characteristics

Statement

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